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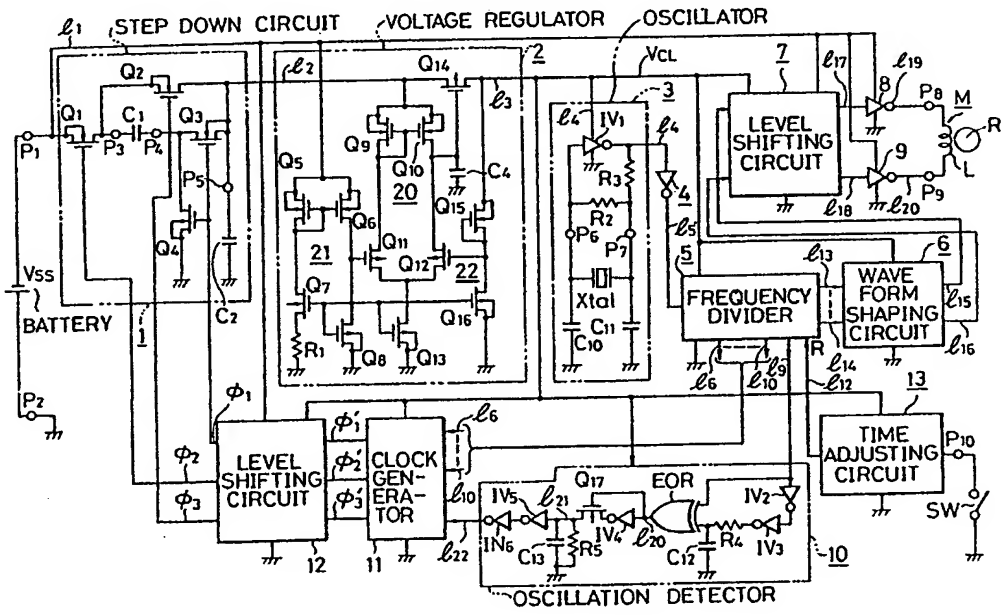
(54) Low Power Consumption Electronic Circuit

(57) A battery voltage is supplied to an electronic circuit such as a watch circuit through a step down circuit (1) constructed of capacitors (C_1, C_2) and switching MISFETs (Q_1 to Q_4). The step down circuit (1) performs a current converting operation as well as a voltage converting operation. It connects the capacitors in series during a first time period and in parallel during a second time period. The output of the step down circuit (1) is stabilized in a voltage regulator (2). A crystal controlled oscillator (3) is powered by the stabilized output of the voltage regulator (2). A clock generator (11) provides clock pulses to a level shifting circuit (12) to control the switching MISFETs. An oscillation detector (10) supplied from the oscillator (3) through a frequency divider (5) detects whether the stabilized voltage has fallen below a predetermined value and controls the operation of the step down circuit (1) through the level shifting circuit (12). Thus, the operating current of the electronic circuit is reduced by a reduction in the operating voltage, thus increasing the life of the battery.

FIG. 1



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This print takes account of replacement documents later filed to enable the application to comply with the formal requirements of the Patents Rules 1978.

FIG. 1

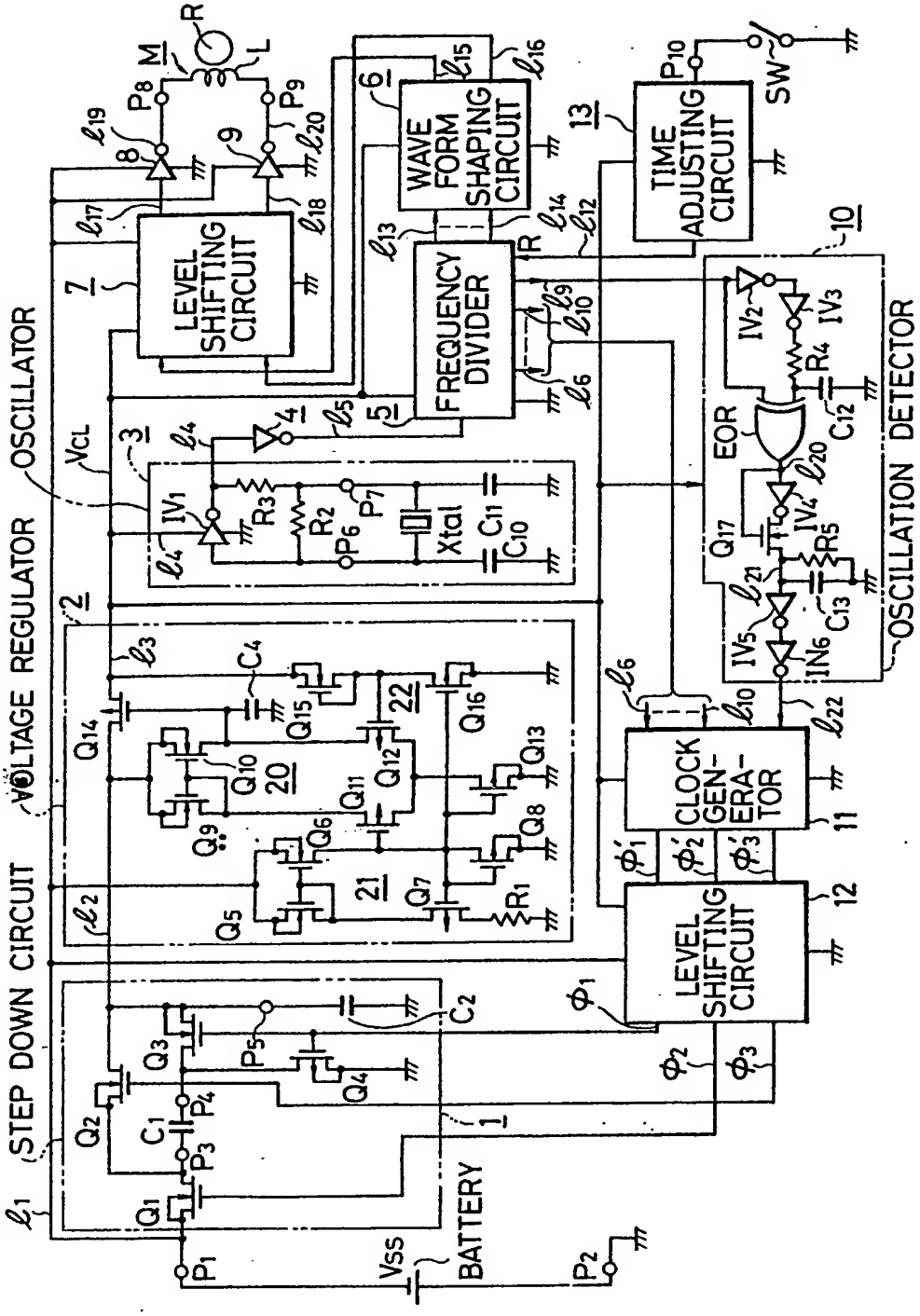
STEP DOWN CIRCUIT
VOLTAGE REGULATOR
OSCILLATOR
OSCILLATION DETECTOR
BATTERY
LEVEL SHIFTING CIRCUIT
FREQUENCY DIVIDER
WAVE FORM SHAPING CIRCUIT
TIME ADJUSTING CIRCUIT
CLOCK GEN-ERA-TOR
LEVEL SHIFTING CIRCUIT
EOR
Xtal
SW
M
R
L
Vss
Vcl

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FIG. 2A

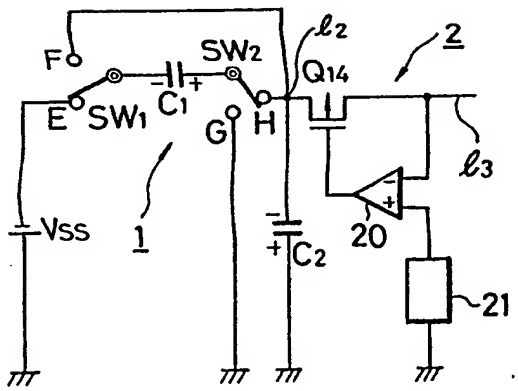

FIG. 2B

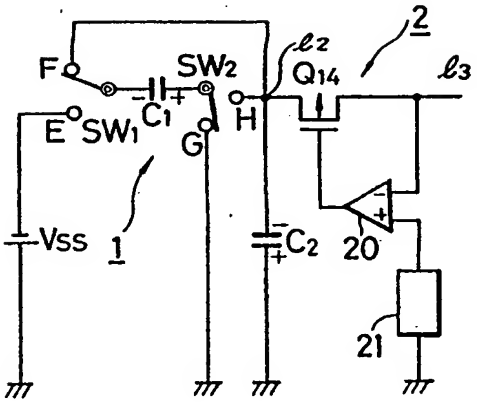

FIG. 3

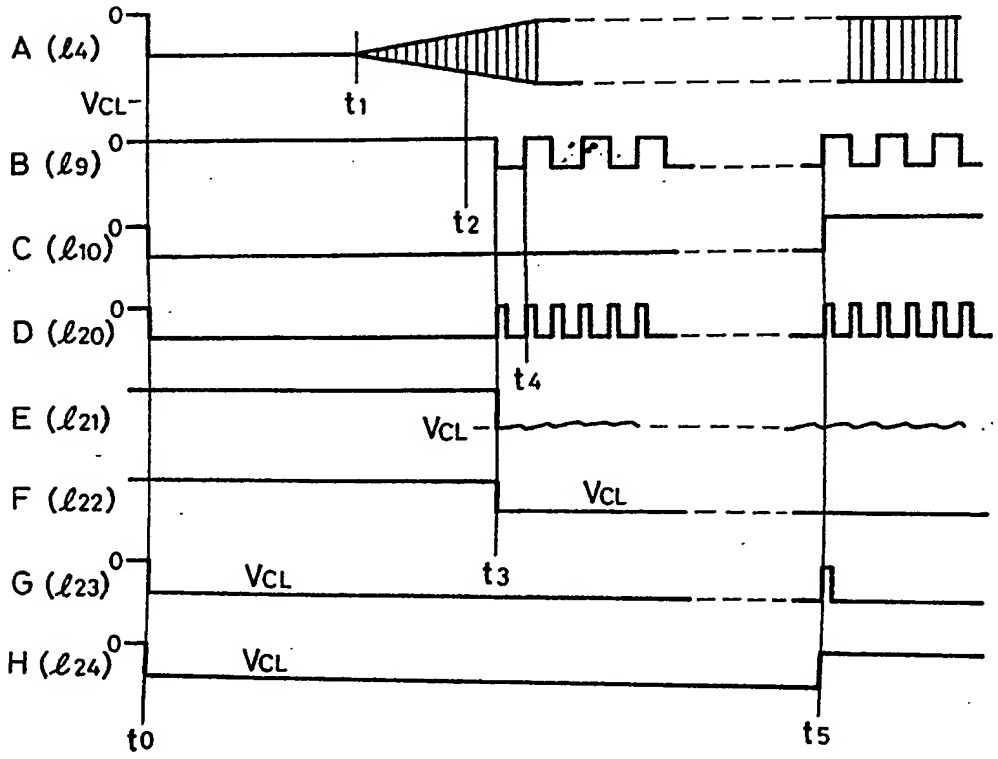

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FIG. 4

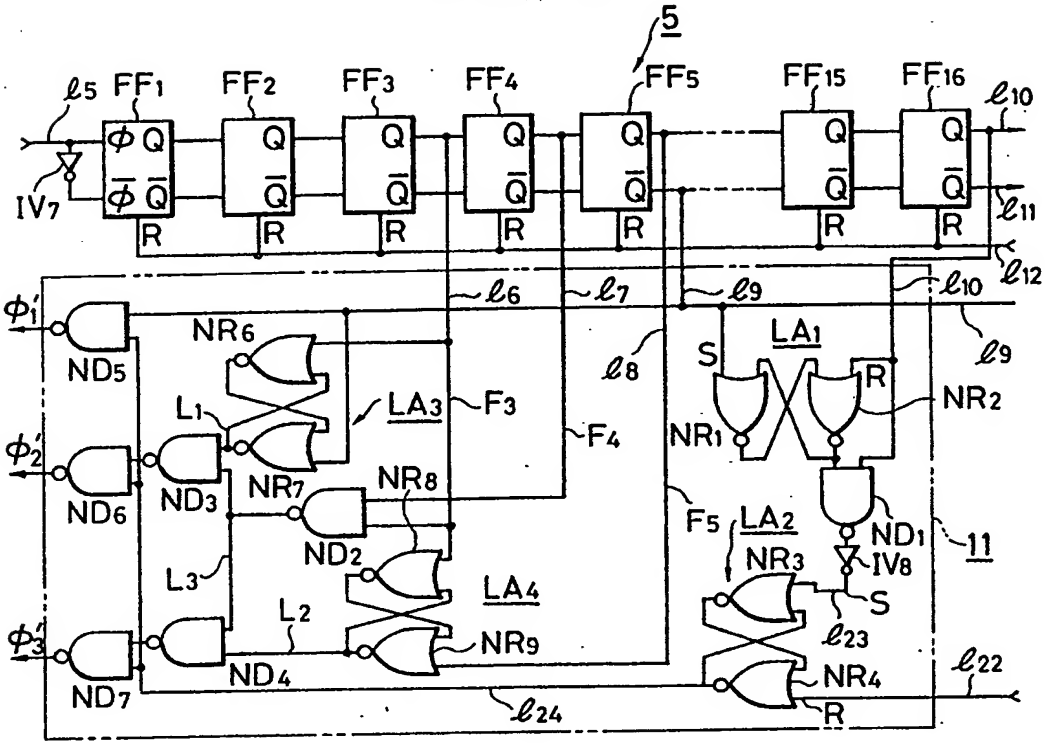

FIG. 5

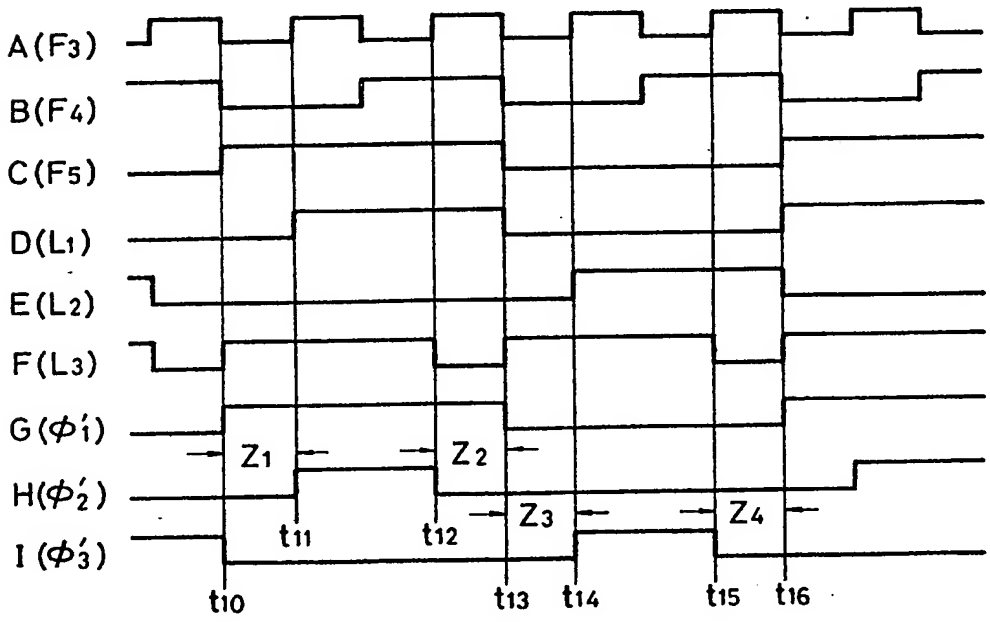

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FIG. 6

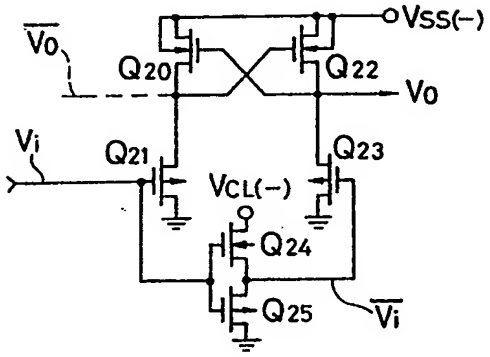

FIG. 7

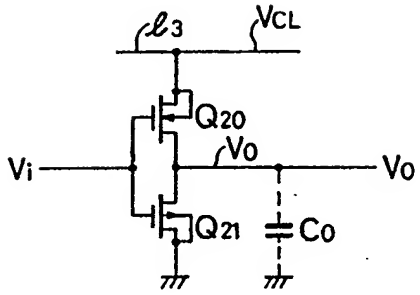

FIG. 8

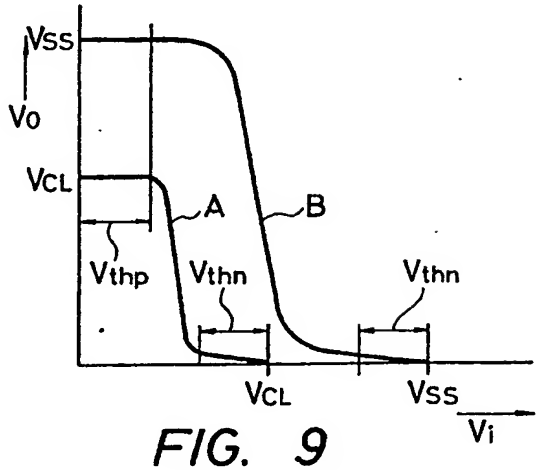

FIG. 9

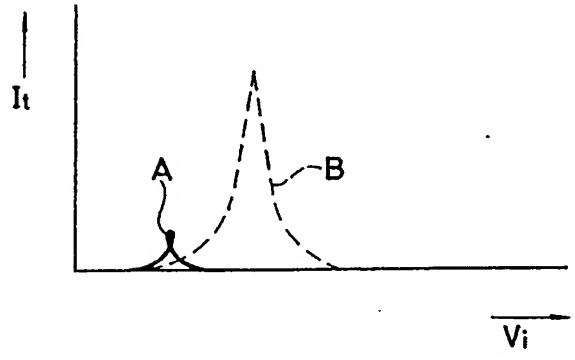

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FIG. 10

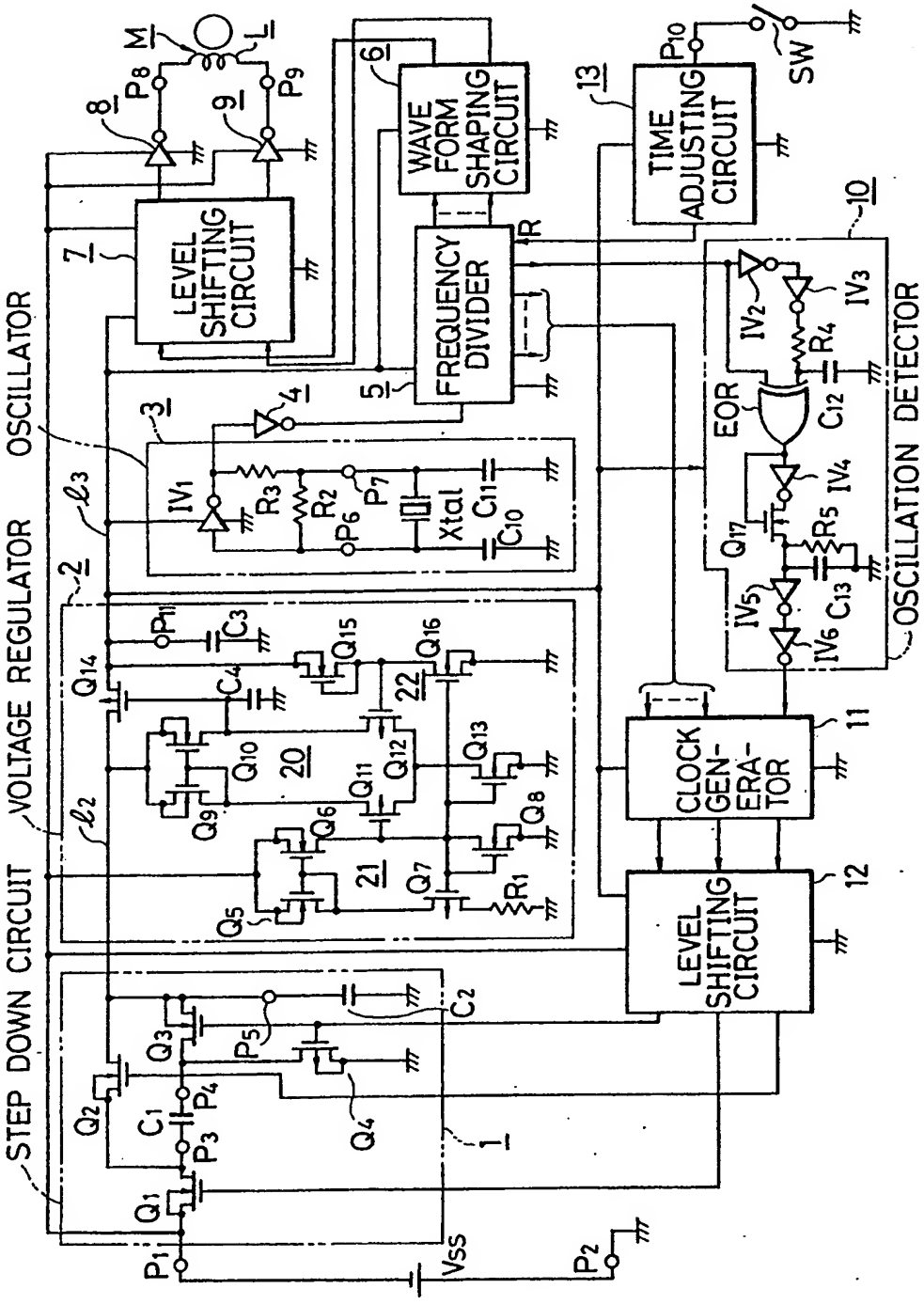

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FIG. 11

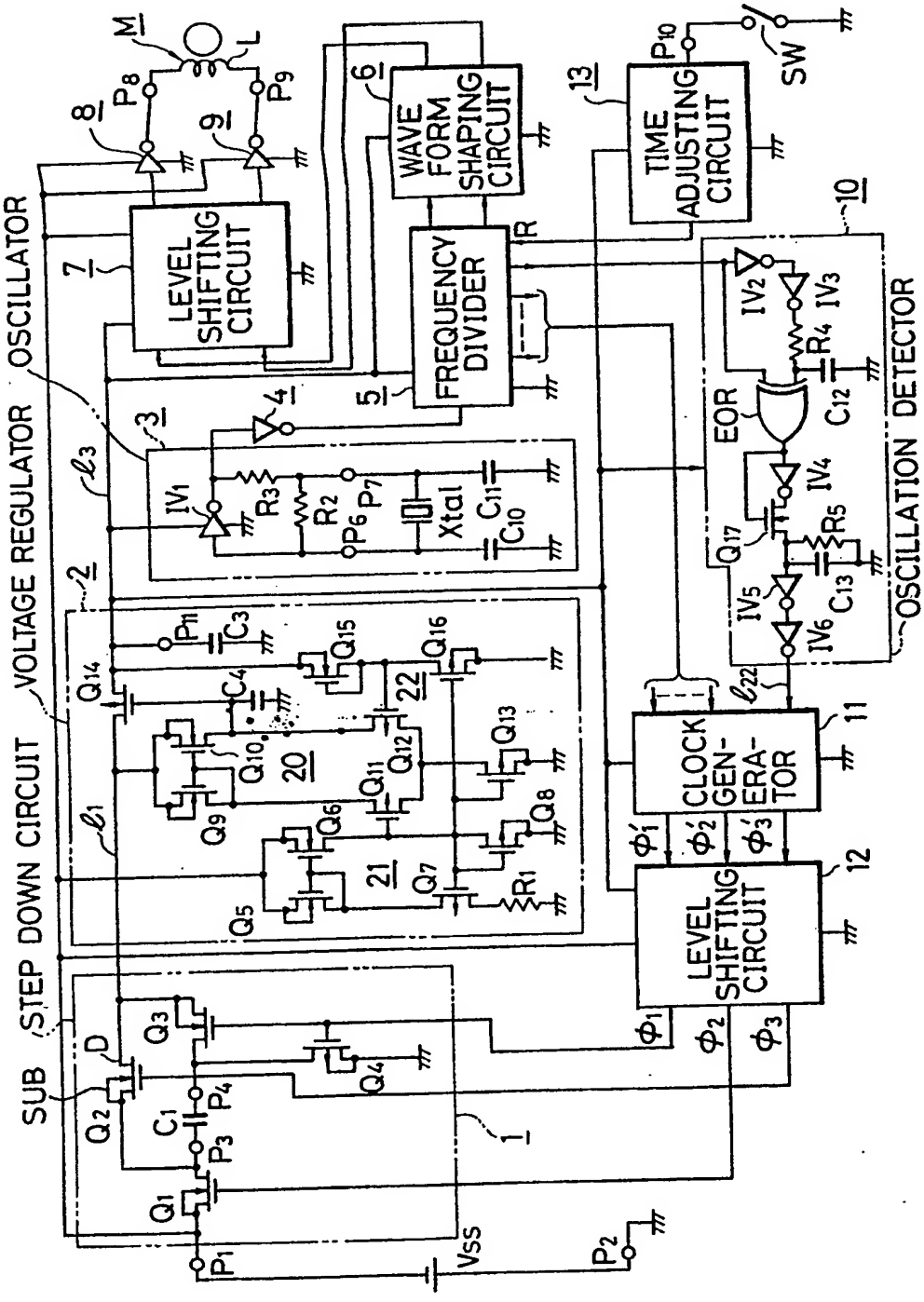

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FIG. 12A

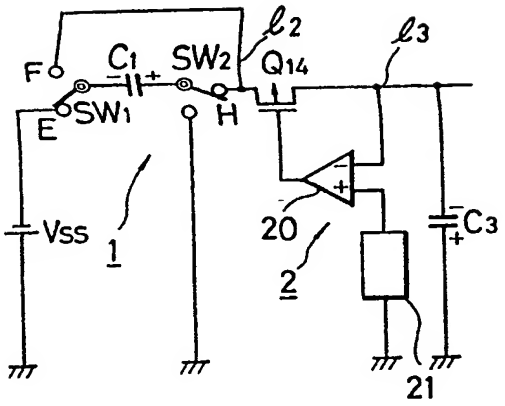

FIG. 12B

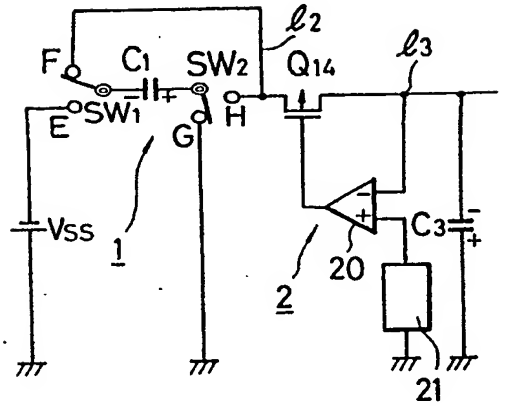

FIG. 13

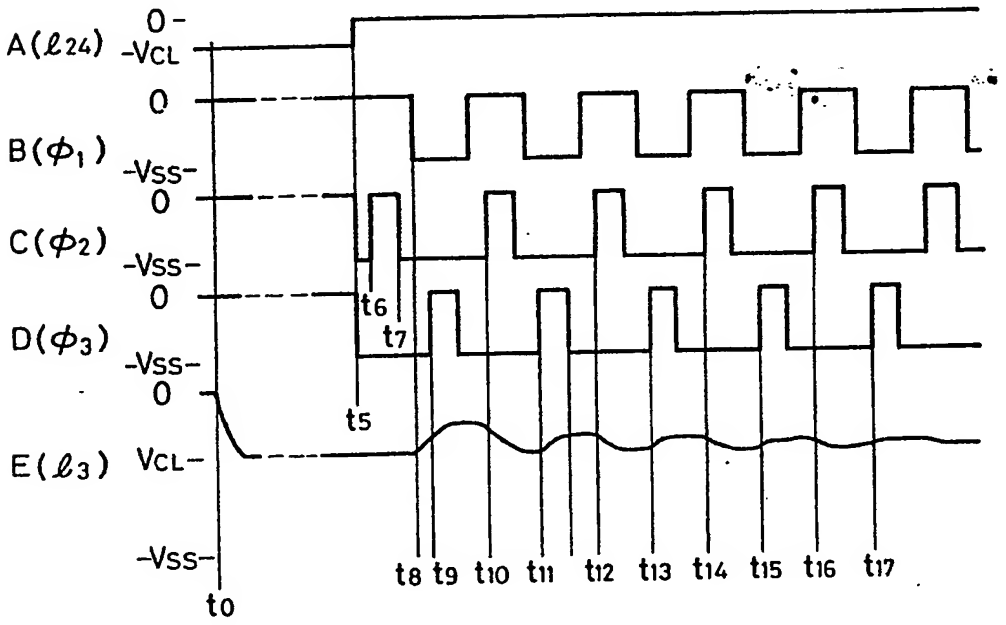

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FIG. 14

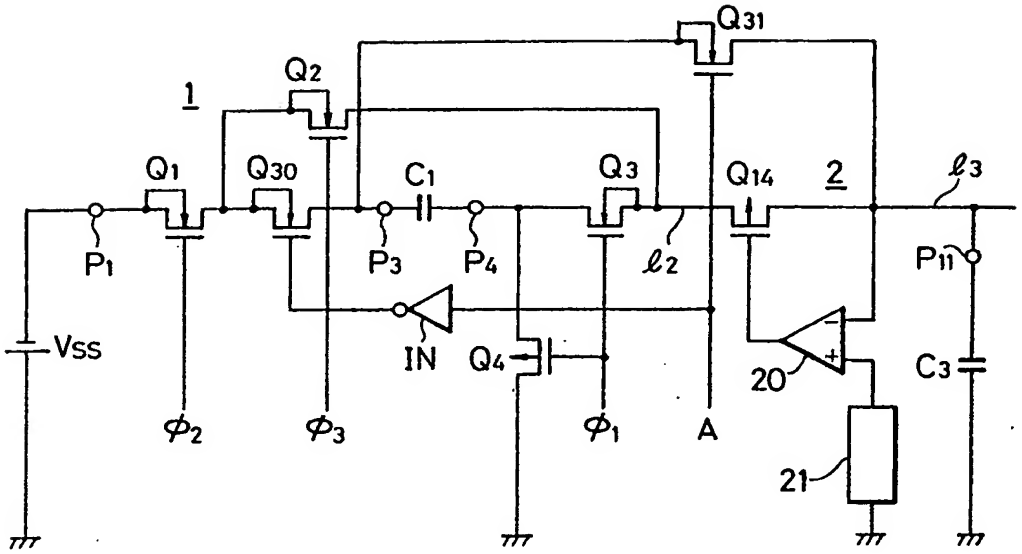

FIG. 15

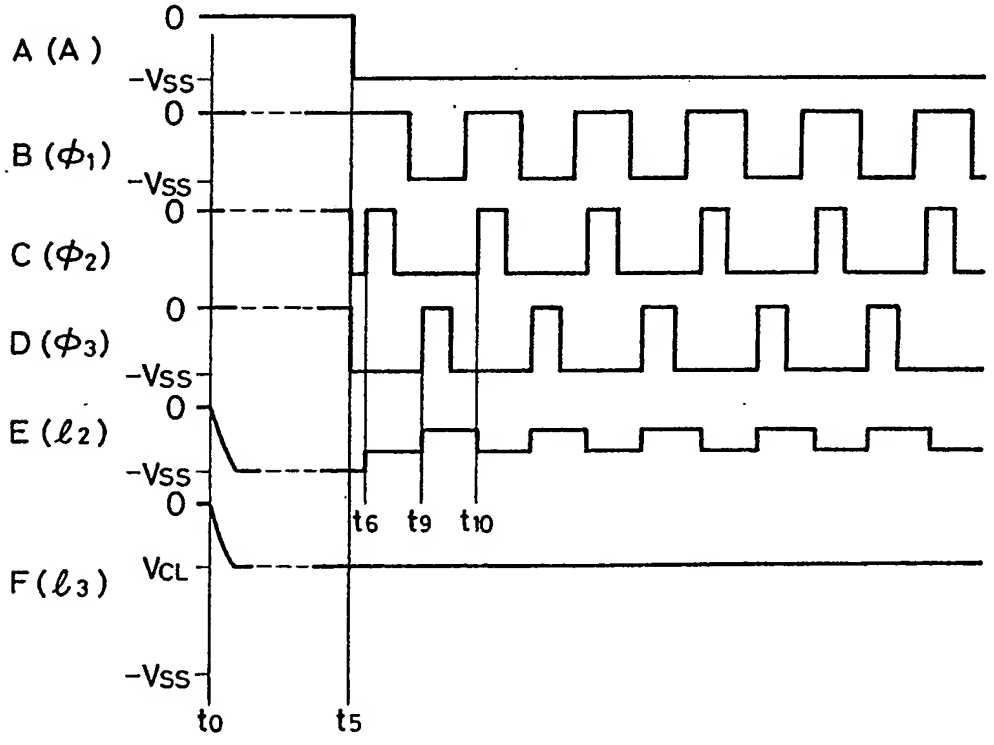

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FIG. 16

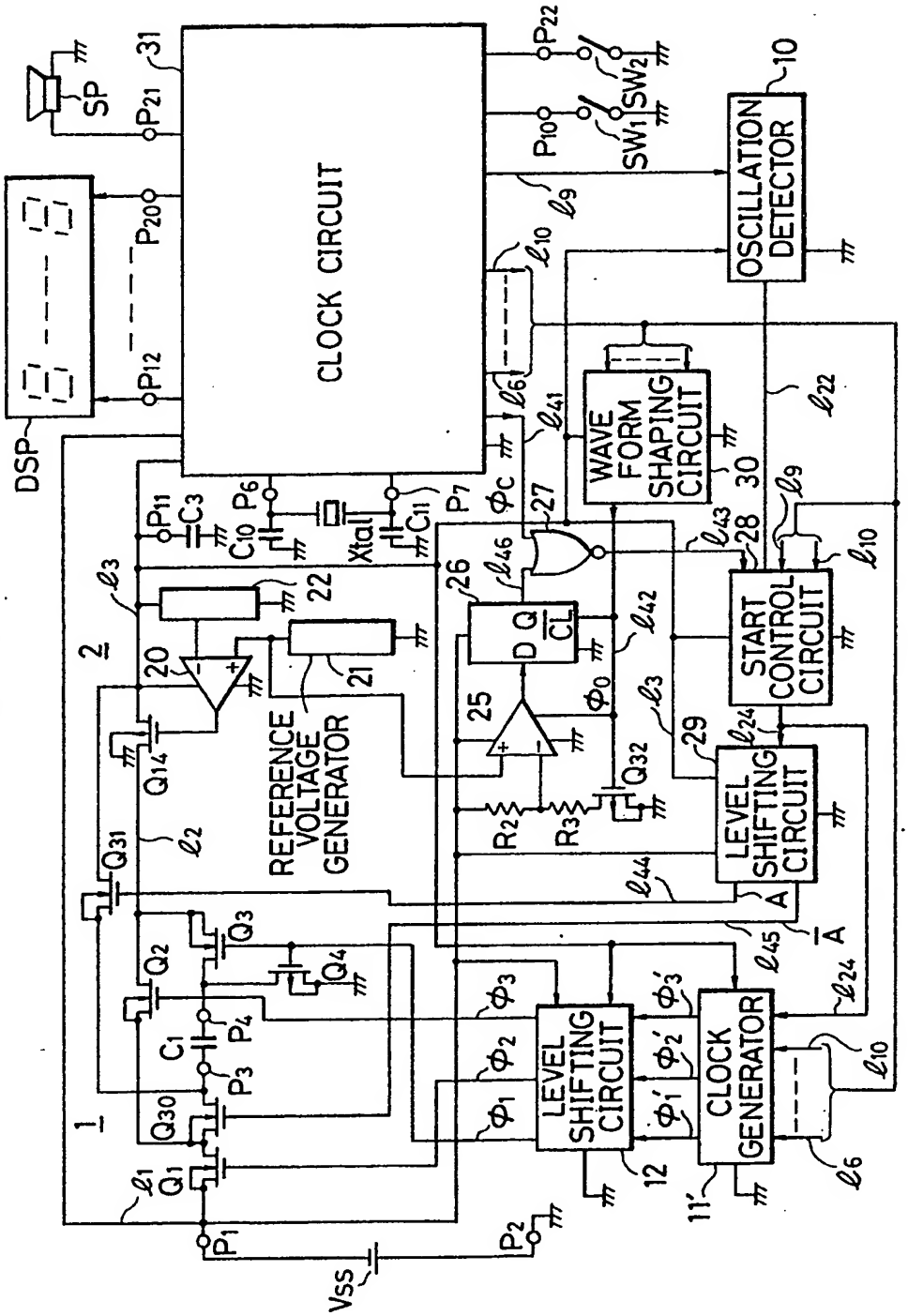

FIG. 17

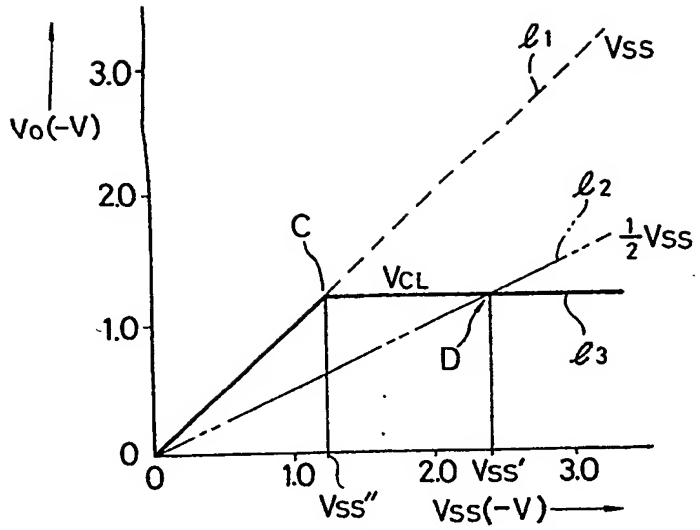
3.0
Vo(-V)
2.0
1.0
0
0
1.0
2.0
3.0
Vss'
Vss''
Vss(-V)
ℓ1
Vss
ℓ2
C
½Vss
VCL
D
ℓ3

FIG. 18

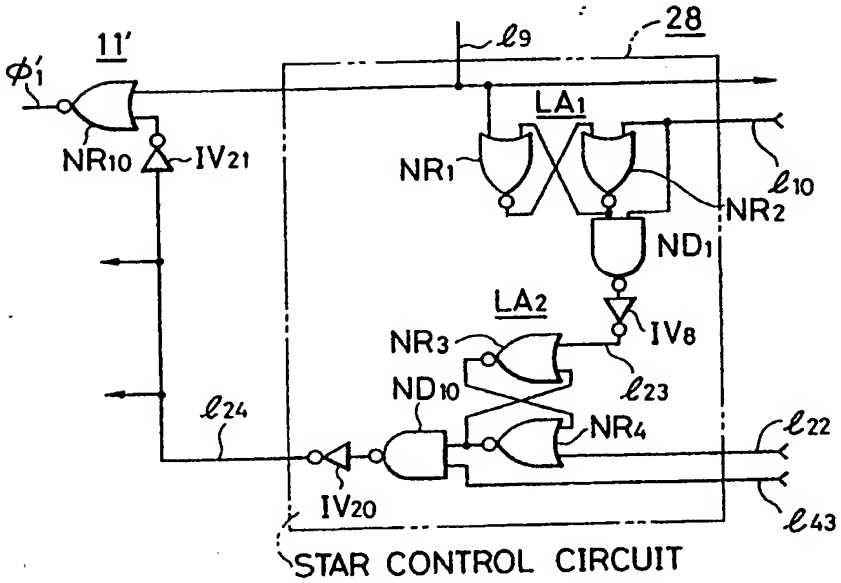
11'
φ'1
NR10
IV21
ℓ9
28
LA1
NR1
NR2
ℓ10
ND1
LA2
IV8
NR3
ND10
ℓ23
NR4
ℓ24
ℓ22
IV20
ℓ43
STAR CONTROL CIRCUIT

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FIG. 19

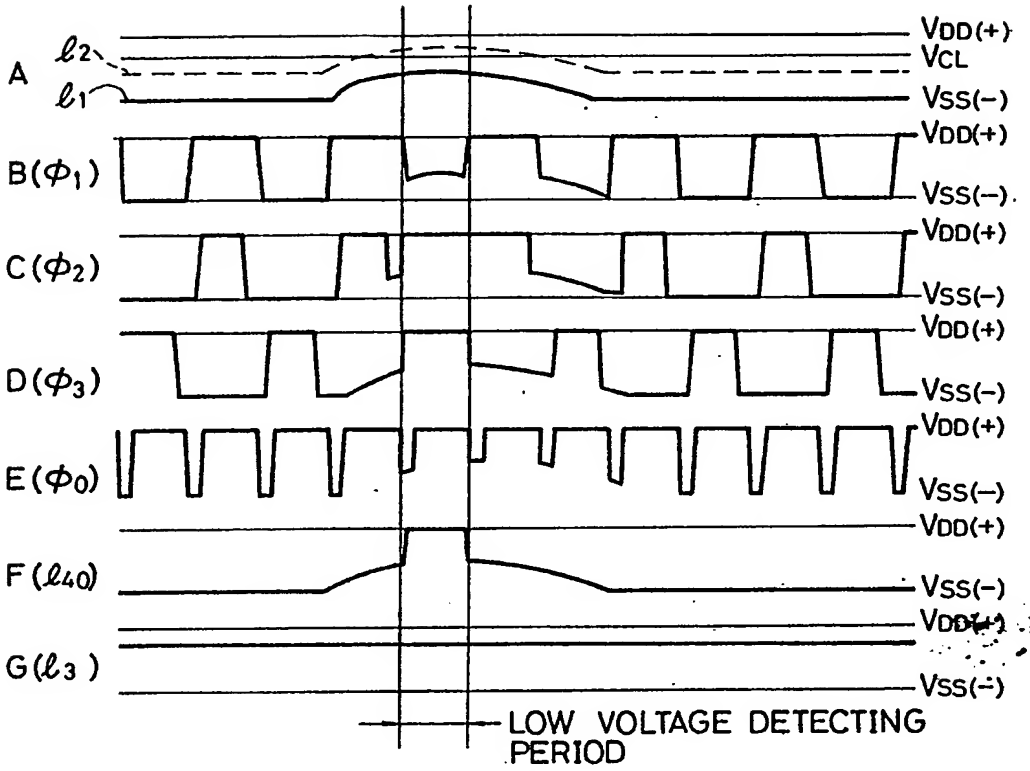

FIG. 20

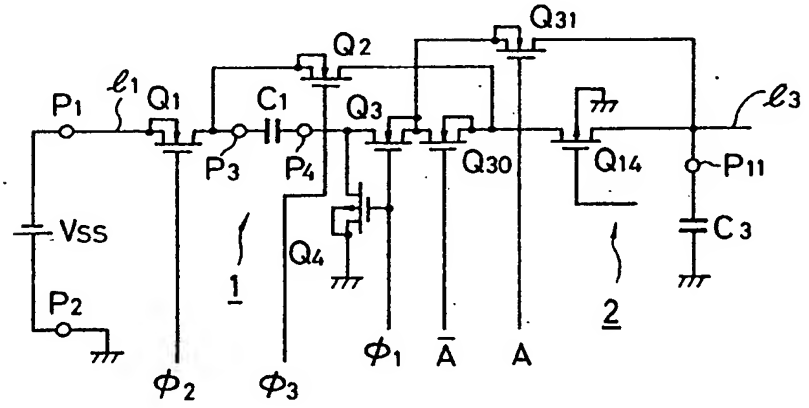

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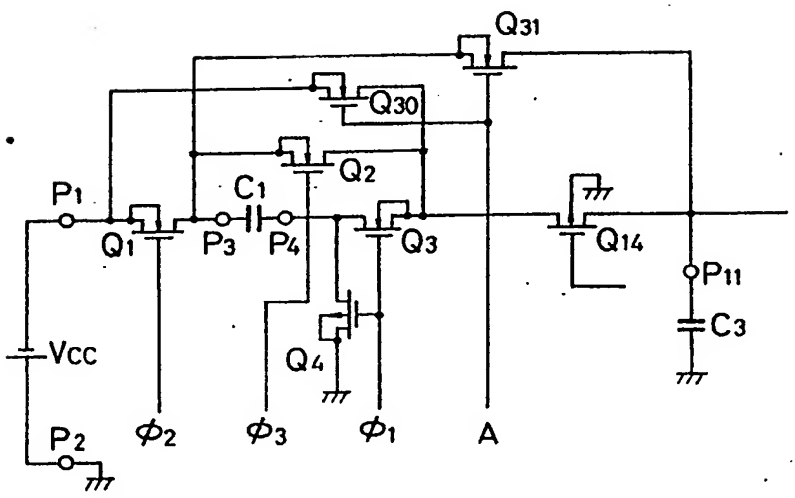
FIG. 21



SPECIFICATION

Low Power Consumption Electronic Circuit

The present invention relates to a low power consumption electronic circuit, and more particularly to a lower power consumption type electronic circuit which is operated by the voltage of a battery.

An electronic circuit such as an electronic watch to be driven by a battery is required to be of low power consumption with a view to increasing the life of the battery.

Generally speaking, a circuit such as an electronic circuit (which will be shortly referred to as an "CMOS circuit"), which is constructed of complementary type insulated gate field effect transistors, can have its current consumption reduced by dropping the voltage supply to be applied thereto.

Consequently, the power to be consumed by an electronic circuit as a whole can be reduced by operating the circuit not with the voltage which is directly supplied from the battery, but with a voltage at a relatively low level which is supplied from a low current consumption voltage regulator.

However, in the above case, between the input and output terminals of the voltage regulator, there appears a voltage at a level which is equal to the difference between the battery voltage and the voltage supplied to the electronic circuit, and a current flows which is substantially equal to that consumed in the electronic circuit.

As a result, a relatively high power consumption takes place in the voltage regulator.

On the other hand, the current to be supplied by the battery is substantially reduced to a quantity equal to the reduction in the current consumed by the electronic circuit. Consequently it is difficult to substantially increase the life of the battery.

It is therefore an object of the present invention to overcome partially or wholly the above referred to disadvantages.

According to the present invention there is provided an electronic circuit including:

(a) a first node arranged to be supplied with a power supply voltage;

(b) a second node;

(c) a step down circuit including a plurality of capacitors and a plurality of switching elements for connecting said capacitors in series during a first time period and in parallel during a second time period, said step down circuit being responsive to the power supply voltage supplied to said first node in order to supply a step down voltage to said second node;

(d) a voltage detector for detecting that said power supply voltage has fallen to a predetermined value; and

(e) a controller reponsive to the detection signal which is supplied by said voltage detector, for controlling the step down circuit.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:—

Figure 1 is a circuit diagram showing a first embodiment of an electronic circuit;

Figures 2A and 2B are circuit diagrams illustrating the operating principle of the electronic circuit shown in Figure 1;

Figure 3 is a series of waveforms illustrating the operation of the circuit shown in Figure 1;

Figure 4 is a detailed logical circuit diagram showing blocks 5 and 11 of Figure 1;

Figure 5 is a series of waveforms illustrating the operation of the circuit of Figure 4;

Figure 6 is a circuit diagram showing a level shifting circuit;

Figure 7 is a circuit diagram showing an inverter circuit;

Figures 8 and 9 are graphs illustrating the characteristic curves of the circuit shown in Figure 7;

Figure 10 is a circuit diagram showing a second embodiment of an electronic circuit;

Figure 11 is a circuit diagram showing a third embodiment of an electronic circuit;

Figures 12A and 12B are circuit diagrams showing the operating principle of the circuit shown in Figure 11;

Figure 13 is a series of waveforms illustrating the operation of the circuit of Figure 11;

Figure 14 is a circuit diagram showing a fourth embodiment of an electronic circuit;

Figure 15 is a series of waveforms illustrating the operation of the circuit of Figure 14;

Figure 16 is a circuit diagram showing a fifth embodiment of an electronic circuit;

Figure 17 is a graph illustrating the characteristic curve of the circuit shown in Figure 16;

Figure 18 is a detailed logical circuit diagram showing the block 28 of Figure 16;

Figure 19 is a series of waveforms illustrating the operation of the circuit shown in Figure 16; and

Figures 20 and 21 are circuit diagrams showing sixth and seventh embodiments of electronic circuits, respectively.

In the first embodiment shown in Figure 1, a stabilized power supply circuit is applied to an analog type electronic wrist watch, the latter only being shown in a block form.

In this embodiment, a lithium battery is used as a battery power supply V_{SS}. It should be noted that a lithium battery has higher storage energy than a silver oxide battery of the same size.

Elements forming the circuit shown are constructed on a single semiconductor substrate by the well-known CMOS ("complementary type metal oxide semiconductor") integrated circuit techniques, except for the battery power supply V_{SS}, capacitors C_1, C_2, C_{10} and C_{11}, a quartz crystal unit X_{tal}, a switch SW and a stepping motor M.

The semiconductor substrate is constructed, although not shown, of n type single-crystalline silicon. On the semiconductor substrate, there are formed p-channel type insulated gate field effect transistors (hereinafter referred to as "MISFETs").

On the semiconductor substrate, moreover, there is formed a p-type well region which in turn is formed with n-channel MISFETs.

The MISFETs of the same conduction type are simultaneously fabricated by semiconductor integrated circuit device fabricating techniques so that they have substantially the same threshold voltages.

It should be noted that the references P_1 to P_{10} appearing in Figure 1 indicate the external terminals of the semiconductor integrated circuit device.

The electronic circuit includes a step down circuit 1 which makes use of the charges on capacitors. The step down circuit 1 comprises: a switching MISFET Q_1; a capacitor C_1; a switching MISFET Q_3 and a capacitor C_2, which are connected in series between the battery voltage terminal P_1 and an earth terminal P_2; a switching MISFET Q_2 which is connected in parallel with a series circuit consisting of the capacitor C_1 and the switching MISFET Q_3; and a switching MISFET Q_4 which is connected in parallel with the series circuit consisting of the switching MISFET Q_3 and the capacitor C_2.

The respective switching MISFETs Q_1 to Q_4 are of the n-channel type, so that the battery voltage supplied to the terminal P_1 has a negative polarity. The MISFETs Q_1 to Q_4 have p-type well regions (although not shown) which are independent of one another are formed as the semiconductor integrated circuit.

In order to minimize the voltage drop due to the substrate effect, the switching MISFET Q_1 has its substrate gate, i.e., its p-type well region electrically connected with the terminal P_1, whereas the switching MISFET Q_2 has its substrate gate electrically connected with a terminal P_3. Likewise, the switching MISFET Q_3 has its substrate gate electrically connected to a terminal P_5.

The semiconductor substrate acting as a common substrate gate for both the p-channel type switching MISFET Q_4 and a variety of p-channel type MISFETs for constructing such various circuits as will be described hereinafter is electrically connected to earth through the terminal P_2.

The capacitors C_1 and C_2 are required to have a relatively large capacitance such as 0.001 μF to 0.1 μF because their respective charge voltages are used as the power supply voltage to be supplied to a voltage regulator 2. However it is difficult to incorporate the capacitors having large values of capacitance into a semiconductor integrated circuit (which will hereinafter be referred to as "IC"). In the embodiment shown, the capacitors C_1 and C_2 are connected to the IC through the external terminals P_3, P_4 and P_5.

The switching MISFETs Q_1 to Q_4 have their gates supplied with the output clock pulses ϕ_1' to ϕ_3' of a clock generator 11 via a level shifting circuit 12.

The switching MISFET Q_1 and Q_3 are simultaneously rendered conductive by clock pulses ϕ_2 and ϕ_1, respectively, whereas the switching MISFETs Q_2 and Q_4 are simultaneously rendered conductive by the clock pulses ϕ_3 and ϕ_1 during a time period different from that whilst the switching MISFETs Q_1 and Q_3 are conductive.

Referring to Figure 2A the capacitors C_1 and C_2 are connected in series with the result that the switching MISFETs Q_1 and Q_3 are rendered conductive. At this state, the capacitors C_1 and C_2 of the series connection are charged by the voltage of the battery supply V_{SS}.

Referring to Figure 2B, the capacitors C_1 and C_2 are connected in series, with the result that the switching MISFETs Q_2 and Q_4 are rendered conductive.

The output voltage of the step down circuit 1 is obtained across the terminals of the capacitor C_2.

By making the values of capacitance of the capacitors C_1 and C_2 relatively large, the output voltage of the step down circuit 1 in the state of Figure 2A takes a value which is substantially determined both by the voltage of the battery supply and by the voltage dividing ratio determined by the capacitors C_1 and C_2, whereas the output voltage of the step down circuit 1 in the state of Figure 2B takes a value which is determined by the combined stored charges of the parallel connected capacitors C_1 and C_2.

By making the values of capacitance of the capacitors C_1 and C_2 equal to each other, the output voltage of the step down circuit 1 in the state of Figure 2A and the output voltage of the step down circuit 1 in the state of Figure 2B can be reduced to a substantially identical value, i.e., substantially one half as high as the voltage of the battery supply V_{SS}.

By the series-parallel converting operations of the capacitors C_1 and C_2, as has been described above, the current which flows from the battery supply V_{SS} is substantially one half as high as the current which flows to the voltage regulator 2.

As will be apparent from the operations of the step down circuit 1, the switching MISFETs Q_1 and Q_3 may be rendered conductive in a manner to complement the switching MISFETs Q_2 and Q_4. For this purpose, the switching MISFETs Q_1, Q_3 and Q_4 can be driven by an identical clock pulse, whereas the switching MISFET Q_2 can be driven by the clock pulse which has a phase opposite to the clock pulse for driving the MISFETs Q_1, Q_3 and Q_4.

In this case, however, by the leading and trailing edge characteristics of the clock pulses, both the switching MISFETs Q_1 and Q_2 and both the switching MISFETs Q_1 and Q_4 are simultaneously rendered conductive in a transient manner so that the following disadvantages result.

First of all, if the switching MISFETs Q_1 and Q_2 are simultaneously rendered conductive, the battery supply V_{SS} and the capacitor C_2 are coupled through those MISFETs Q_1 and Q_2. As a result, the charging voltage of the capacitor C_2 is raised to a higher value than that which is determined by the voltage dividing ratio of the

capacitors C_1 and C_2. In accordance with the rise in the charging voltage of the capacitor C_2, the voltage to be supplied to the voltage regulator 2 is raised so as to increase the power loss in itself.

Likewise, when the switching MISFETs Q_1 and Q_4 are simultaneously rendered conductive, the charging voltage of the capacitor C_1 is raised. As a result of the rise of this capacitor C_1, the charging voltage of the capacitor C_2 is raised when the parallel converting operation is started. As a result, the power loss in the voltage regulator 2 is increased.

In order to prevent the increase in the power loss, the clock pulses ϕ_1' to ϕ_3' are made to have such timings as are shown in Figures 5G to 5I, respectively.

When the clock pulse ϕ_1 is raised to a high level at the time t_{10}, so as to be substantially equal to earth potential, the clock pulse ϕ_2' is raised to a high level at a time t_{11} after a time period Z_1 has elapsed from the time t_{10}. When a time period Z_2 has elapsed after the clock pulse ϕ_2' has fallen to a low level which is substantially equal to the voltage V_{CL}, the clock pulse ϕ_1' falls to a low level. Likewise, when a time period Z_3 has elapsed after the clock pulse ϕ_1' has fallen to the low level, the clock pulse ϕ_3 is raised to the high level. When a time period Z_4 has elapsed after the clock pulse ϕ_3' has fallen to the low level, the clock pulse ϕ_1' is raised again to the high level.

The voltage regulator 2 receives the output voltage of the step down circuit 1 through its input line l_2 supplies a constant voltage at its output line l_3. The output voltage of the voltage regulator 2 is set to such a value as is dropped to the vicinity of the operating lower limit voltage of each electronic circuit.

The nominal electromotive voltage of the lithium battery is about 3 V so that the output voltage of the step down circuit is accordingly set to about 1.5 V. Consequently, the operating lower limit voltage of the various circuits is set to 1.2 V.

The voltage regulator 2 comprises: a p-channel type control MISFET Q_{14} which has its drain coupled to the input line l_2 and its source coupled to the output line l_3; a differential amplifier 20 for supplying a control voltage to the gate of the control MISFET Q_{14}; a reference voltage generator 21 for supplying a reference voltage to the difference amplifier 20; and a level shifting circuit 22.

The reference voltage circuit 21 comprises MISFETs Q_5 to Q_8 and a resistor R_7.

The MISFET Q_8 has its gate and drain connected to generate such a constant voltage between its drain and source as substantially corresponds to the threshold voltage thereof. This constant voltage is supplied to the gate of the MISFET Q_7. This MISFET Q_7 establishes at its drain a drain current at such a level as is determined by both the constant voltage supplied to the drain thereof and the resistance of a resistor R_1 connected to the source thereof.

The drain current of the MISFET Q_7 flows to the MISFET Q_5 forming a part of a current mirror circuit so that a drain current for biasing the MISFET Q_8 is accordingly supplied from the drain of the MISFET Q_8.

The output voltage of the reference voltage circuit 21, i.e., the drain voltage of the MISFET Q_8 is used as the gate bias voltage of the differential and constant current MISFETs Q_{11} and Q_{13} of the differential amplifier 20 and the constant current MISFET Q_{16} of the level shifting circuit 22.

It should be noted that in the reference voltage circuit 21, immediately after the battery supply V_{SS} is connected between the terminals P_1 and P_2, the MISFET Q_6 has its gate electrode potential maintained at earth potential for a predetermined time by the stray capacitance of the circuit. The MISFET Q_6 is rendered conductive by the voltage between its gate and source. As a result, the reference voltage circuit 21 is started when the battery supply V_{SS} is connected.

The level shifting circuit 22 comprises: the constant current MISFET Q_{16}; and a level shifting MISFET Q_{15} connected in diode configuration so as to generate a voltage at a level which has fallen by an amount equal to the threshold voltage of the level shifting MISFET Q_{15} from the voltage at the output line l_3.

The differential amplifier 20 comprises: the differential MISFETs Q_{11} and Q_{12}; a constant current MISFET Q_{13} which is connected to the common sources of the differential MISFETs Q_{11} and Q_{12}; and MISFETs Q_9 and Q_{10} which are connected to the drains of the MISFETs Q_{11} and Q_{12} in order to form a current mirror circuit.

In the differential amplifier 20, the common gates of the differential MISFETs Q_{11} and Q_{12} and the drain of the differential MISFEt Q_{12} constitute a non-inverting input terminal, an inverting input terminal and an output terminal, respectively.

A constant voltage substantially equal to the threshold voltage of the MISFET Q_8 is applied to the gate of the MISFET Q_{11}, which acts as the non-inverting input terminal of that differential amplifier 20, whereas the stabilized output voltage V_{CL} of the MISFET Q_{12}, which acts as the inverting input terminal, is applied through the MISFET Q_{15} to the gate of the MISFET Q_{12}, which acts as the inverting input terminal.

The differential amplifier 20 controls the impedance of the MISFET Q_{14} such that the voltage having its level shifted by the threshold voltage of the MISFET Q_{15} becomes equal to the constant voltage generated by the MISFET Q_8.

As a result, the stabilized output voltage V_{CL} to be generated at the output line l_3 has a value equal to the sum of the voltage between the drain and source of the MISFET Q_8 and the voltage having its level shifted by the MISFET Q_{15}.

The stabilized output voltage V_{CL} is set at a value close to the operating lower limit voltage of the circuit both by suitably designing the respective sizes of the MISFETs Q_8 and Q_{15} and by setting the bias current voltage thereof.

Incidentally, as a result that all the respective MISFETs of the circuits described above, have

mutually similar threshold voltages, the stabilized output voltage V_{CL} is automatically set to a value which is suitable for the supply voltage for the circuits irrespective of both the dispersion in the absolute values of the threshold voltages of the respective MISFETs and fluctuations due to temperature.

In the case where the operating lower limit voltage of the above described circuits is increased by an increase in the threshold voltage of the p-channel MISFETs of the above circuits, the output voltage of the reference voltage circuit 21 is increased by an increase in the threshold voltage of the p-channel MISFET Q_8. As a result, a properly raised voltage V_{CL} is supplied from the voltage regulator 2. Likewise, in the case where the operating lower limit voltage of the above circuits is increased by an increase in the threshold voltage of the n-channel MISFET of the above circuits, the voltage having its level shifted by the level shifting circuit 22 is increased by an increase in the threshold voltage of the n-channel MISFET Q_{15}. As a result, the output voltage V_{CL} is properly raised.

Likewise, in the case where the operating lower limit voltage of the above circuits is reduced, the voltage V_{CL} is also properly reduced.

The circuits 20 to 22 can be operated by a very small bias current such as 10 nA, by suitably designing their respective MISFETs Q_5 to Q_{18} and the resistor R_1.

The supply voltage for operating the differential amplifier 20 is supplied from the step down circuit 1, whereas the power supply voltage for operating the reference voltage circuit 21 is supplied directly from the battery source V_{SS}.

If the reference voltage circuit 12 is constructed such that it is operated directly by the battery supply V_{SS}, as has been described hereinbefore, a constant voltage to be used as a satisfactory reference voltage can be supplied from the reference voltage circuit 21 even if the battery voltage is reduced by the consumption from the battery. Incidentally, the reference voltage circuit 21 is sufficient to generate a constant voltage at a relatively low level which corresponds to the level of the threshold voltage of the MISFET Q_8. In order to further reduce the power consumption of the reference voltage circuit 21, therefore, the supply voltage may be obtained from the step down circuit 1 in similar manner to the differential amplifier 20.

It should be noted that a capacitor C_4, which is connected between the gates of the MISFET Q_{14} and earth, is provided partly to prevent the voltage regulator 2 from oscillating and partly to prevent the fluctuations in the step down voltage generated by the step down voltage 1 from being transmitted to the gate of the MISFET Q_{14} by the overlap capacitance (i.e., the drain-gate capacitance), which exists between the drain and gate of the MISFET Q_{14}, whereby the stabilized output voltage V_{CL} is prevented from fluctuating. That capacitance is set to a relatively large value such as 20 pF to 40 pF.

The stabilized output voltage V_{CL} is used as the supply voltage for circuits to be described in the following.

The electronic circuits further include an oscillator 3 which is designed to generate a reference frequency signal of 32.768 KHz.

The oscillator 3 comprises an inverter IV_1 acting as an amplifier; an oscillation stabilizing resistor R_3; a bias resistor R_2; a quartz crystal unit X_{tal}; and capacitors C_{10} and C_{11}.

Referring to Figure 7, the inverter IV_1 comprises an n-channel type MISFET Q_{20} and a p-channel type MISFET Q_{21}, and is operated by the supply voltage V_{CL} which is supplied from the voltage regulator 2.

The capacitors C_{10} and C_{11} for determining the oscillation frequency together with the quartz crystal unit X_{tal} are selected from those, which have capacitances of a predetermined temperature coefficient, with a view to reducing the temperature coefficient of the oscillation frequency and are formed as external elements from the IC.

The inverter in Figure 7 is designed to have an output voltage characteristics against an input voltage V_I which is indicated by a curve B of Figure 8 if its operating voltage is made equal to the battery voltage V_{SS}.

The p-channel type MISFET Q_{21} is rendered conductive when the input voltage V_I is made higher than the threshold voltage V_{thp} thereof, whereas the n-channel type MISFET Q_{21} is rendered conductive when the input voltage V_I becomes lower than the value which is calculated by subtracting the threshold voltage V_{thn} from the voltage V_{CL} on the line l_3. As a result, a current flows, as indicated by a broken curve B of Figure 9, through the source-drain paths of the series connected MISFETs Q_{20} and Q_{21} in accordance with the change in the input voltage V_I.

On the other hand, in the case where the conductive and non-conductive states of the MISFETs Q_{21} and Q_{22} are inverted subsequent to the state, at which the potential at an output node N_o is held substantially at earth potential, by the conductive state of the MISFET Q_{21} and then by the non-conductive state of the MISFET Q_{20}, the charging current flows into a capacitor C_o, which is coupled to the output node N_o, through the MISFET Q_{20} from the line l_3.

As a result, the power to be consumed by the inverter shown in Figure 7 is determined by both the through current, which is established as a result that the MISFETs Q_{20} and Q_{21} are simultaneously rendered substantially conductive, and the charging and discharging currents to and from the capacitor C_o.

The range of the input voltage V_I, within which the through current flows in accordance with the reduction in the voltage V_{CL} on the line l_3, is reduced, and the level of the through current itself is reduced.

Moreover, since the changing range of an output voltage V_o is reduced in accordance with the voltage V_{CL} on the line l_3, the charging and

discharging currents which flow through the capacitor C_0 are reduced.

As a result, the inverter of Figure 7 has its power consumption reduced.

It should be noted that a curve A of Figure 8 illustrates the output voltage characteristics against the input voltage of the inverter in the case where the output voltage V_{CL} of the voltage regulator 2 is supplied to the line l_3, whereas a solid curve A of Figure 9 illustrates the through current waveforms when the inverter is designed to have the characteristics of the curve A of Figure 8.

The oscillator 3 of Figure 1 generates a reference frequency signal having a waveform similar to a sine wave. This reference frequency signal is supplied to an inverter 4 acting as a waveform shaping circuit which is receptive to the voltage V_{CL} on the line l_3 as the supply voltage.

As a result, the inverter 4 generates the reference frequency signal, which has its waveform shaped as the pulse signal, in accordance with the sinusoidal reference frequency signal supplied by the oscillator 3.

The output signal of the inverter 4 is supplied through a line l_5 to the input terminal of a frequency divider 5.

As shown in Figure 4, this frequency divider 5 comprises sixteen flip-flops FF1 to FF16 connected in series and an inverter IV_7.

Each of the flip-flops FF1 to FF16 is designed so that the output signals at output terminals Q and $\overline{Q}$ are inverted in synchronism with the trailing edge of the clock signal which is applied to the clock input terminal Ø thereof.

As a result, in accordance with the reference pulse signal of 32.768 KHz, which is supplied through the line l_5 from the inverter 4, a pulse signal of 16.384 KHz is generated at the output terminal of the flip-flop FF1, and a pulse signal of 8.192 KHz is generated at the output terminal of the flip-flop FF2. Likewise, a pulse signal of 0.5 Hz is generated at the output terminal of the flip-flop FF16 at the final step.

The output pulse signals at the respective frequencies, which are output from the frequency divider 5, are supplied through a line l_{13} or l_{14} to a waveform shaping circuit 6.

This waveform shaping circuit 6 is provided to generate a pulse signal for driving a bipolar drive stepping motor M and consists of a suitable gate circuit, although not shown, which is receptive to the voltage V_{CL} on the line l_3 as the supply voltage.

The waveform shaping circuit 6 supplies a pulse signal which has its level raised substantially to the voltage V_{CL} and which is fed alternately every other second to lines l_{15} and l_{16}. In order to reduce the average of the drive current to flow into the bipolar drive stepping motor M, the pulse signals of the lines l_{15} and l_{16} have their levels raised to a high one during their one period, e.g., for 15.6 ms.

It should be noted that the signal level, which is reduced substantially to earth potential in a manner to correspond to the fact that the supply voltage supplied to the external terminal P_1 of the IC has a negative polarity, is deemed to be high, and the signal level, which is changed substantially to the supply voltage level of the circuit, it deemed to be low.

The output pulse signal of the waveform shaping circuit 6 is supplied through a level shifting circuit 7 to output buffer circuits 8 and 9.

The output pulse signals of the output buffer circuits 8 and 9 are supplied through the external terminals P_8 and P_9 to the energizing winding L of the bipolar drive stepping motor M.

As a result that the output voltages of the output buffer circuits 8 and 9 are reduced from the high level to the low level for the period of 15.6 ms every other second, the drive current having its polarity inverted for one second is supplied to the energizing winding L.

As a result, the rotor R of the stepping motor M is rotated a predetermined rotational angle every second. The gear trains of the watch (not shown) are driven once a second by the rotor R.

The bipolar drive stepping motor M usually requires such a drive current as is considerably larger than the operating current of the respective circuits.

The output buffer circuits 8 and 9 are so designed that they operate in a manner to use the battery voltage supply V_{SS} as a direct supply.

By means of the connections described above, the load current of the voltage regulator 2 can be reduced, and the drive current of the stepping motor M is not supplied from the voltage regulator 2 so that the voltage V_{CL} on the line l_3 can be sufficiently stabilized notwithstanding that the drive current is intermittently generated.

Moreover, the supply voltage of the output buffer circuits 8 and 9 is freed from the influences due to the voltage drop which takes place in the voltage regulator 2. Consequently, even at the state in which the voltage of the battery supply V_{SS} has been relatively reduced, a sufficiently large drive current can be supplied to the stepping motor M through the output buffer circuits 8 and 9.

These output buffer circuits 8 and 9 consist of a complementary type inverter as is shown in Figure 7. When the inverter of Figure 7 is operated by the battery voltage supply V_{SS}, the input voltage V_I at the level of the battery voltage supply V_{SS} is required for rendering the n-channel type MISFET Q_{20} sufficiently non-conductive.

The pulse signal supplied from the waveform shaping circuit 6 to the lines l_{15} and l_{16}, as described above, is set to have its low level the same as that of the stabilized constant voltage V_{CL}. Accordingly, the level shifting circuit 7 is designed so as to shift the level of the low level output signal of the waveform shaping circuit 6 to the low level signal at the voltage level of the battery voltage supply V_{SS}.

As shown in Figure 6, the level shifting circuit 7 comprises: MISFETs Q_{20} to Q_{23} which are

operated by using the voltage V_{SS} as the supply voltage; and MISFETs Q_{24} and Q_{25} which are operated by using the voltage V_{CL} as the supply voltage so as to generate an inverted signal in response to the input voltage V_I.

The electronic circuits also include a time adjusting circuit 13, which is responsive to the signal from a key switch SW through an external terminal P_{10} in order to supply a line l_{12} with a signal for resetting the frequency divider 5. The time adjusting circuit 13 is designed to feed the line l_{12} with a high level signal for a predetermined time irrespective of the operation of the key switch SW when the battery voltage supply is connected.

The clock generator 11 generates the clock pulses ϕ_1' to ϕ_3' for operating the step down circuit 1, as has been described in the above. In an alternative form, the clock generator 11 can be modified so that it consists of: an oscillator which is made operative to generate a reference clock by using the battery voltage supply V_{SS} as a direct supply; and a logical circuit which is receptive to the output of the oscillator.

In the present embodiment shown in Figure 1, the reference clock 11 is supplied from the frequency divider 5. It is therefore unnecessary to provide the oscillator in the clock generator 11 and this prevents both the undesired increase in the power consumption by the circuit and in the number of the circuit elements required in the semiconductor integrated circuit device.

Moreover, the clock generator 11 is designed so that it receives the voltage, which is dropped by the voltage regulator, as the supply voltage in place of the voltage of the battery voltage source V_{SS}.

Since the low level of the output clock signal of the clock generator 11 is not sufficient for switching the MISFETs Q_1 and Q_2 of the step down circuit 1, the level shifting circuit 12 is provided.

The level of shifting circuit 12 is designed in similar manner to the level shifting circuit 7 as is shown in Figure 6. The level shifting circuit 12 is designed to have a relatively simplified construction in order to reduce the power consumption.

On the contrary, the clock generator 11 is designed to have such a relatively complex construction as to consume relatively high power, as is apparent from the detailed circuit shown in Figure 4.

Consequently, the construction, in which the supply voltage of the clock generator 11 is dropped by the step down circuit 1 and the voltage regulator 2 as in the above, can effect a lower power consumption than the construction, in which the level shifting circuit 12 is dispensed with by operating the clock generator 11 directly with the voltage from the source of battery voltage V_{SS}.

In the case where the output voltage of the step down circuit 1 is zero, the oscillator 3 is not operated so that no clock pulses are generated for supplying to the step down circuit 1.

In order that the voltage necessary for the operation of the oscillator may appear on the line l_3 when the battery voltage supply V_{SS} is connected, the necessary voltage has to be supplied by the step down circuit 1 even if the oscillator 3 is left inoperative.

The switching MISFETs Q_1, Q_2 and Q_3 have their gate potentials raised to the high level such as earth potential, at the instant when the battery is connected by capacitors such as stray capacitances which are connected between their respective gates and earth, so that they are rendered conductive. As a result, the input line l_2 of the voltage regulator 2 is supplied with the voltage. However, if at least one of the switching MISFETs Q_1 and Q_2 is rendered non-conductive before the voltage to be supplied to the input line l_2 is raised to the desired level, a signal generating circuit such as the oscillator is not supplied with a sufficient operating voltage.

In order that the voltage at a desired level may be supplied to the line l_2 when the battery voltage supply V_{SS} is connected, the switching MISFETs Q_1 to Q_3 of the step down circuit 1 are positively and simultaneously rendered conductive.

As a result, a voltage substantially equal to that of the battery voltage supply V_{SS} is supplied from the step down circuit 1 so that a predetermined voltage is accordingly supplied from the voltage regulator 2.

The start state, i.e., the state, at which the switching MISFETs Q_1 to Q_3 are simultaneously rendered conductive, is continued for a period until the oscillator 3 is rendered sufficient oscillatory. As a result, the operation of the respective circuits of Figure.1 are ensured.

In order to achieve the starting state, a latch circuit is provided and designed to be set by the rise of the supply voltage V_{SS} when the battery is connected, and to be reset by the rise of the output signal at a predetermined output step of the frequency divider 5, whereby the switching MISFETs Q_1 to Q_3 are simultaneously rendered conductive on the basis of the output signal of the latch circuit.

In the oscillator 3 which is operated by a relatively low voltage it should be taken into consideration that it takes a relatively long time for the oscillator 3 to be brought into a sufficiently stable oscillator state after the voltage supply has been connected and that the operation of the oscillator 3 midway of the start of the oscillating operation is made relatively unstable by fluctuations in the supply voltage.

In the case where the starting state is ended, the output voltage of the step down circuit 1 starts to drop from a voltage substantially equal to the voltage of the battery supply V_{SS}. In fact, the voltage regulator 2 is not a fully stabilized circuit so that its output voltage is effected by changes in the input voltage. The output voltage of the voltage regulator 2 is slightly reduced in accordance with the reduction in the output voltage of the step down circuit 1 and fluctuates

in accordance with such fluctuations in the output voltage of the step down circuit 1 as accompany the start of the switching operation of the switching MISFETs Q_1 to Q_4.

As a result, the operation of the oscillator 3 may become unstable immediately after the starting state has ended. If the period of the clock pulse applied to the step down circuit 1 is changed in accordance with the unstableness in the oscillations, the changing amplitude of the output voltage of the step down circuit 1 is accordingly increased, and the operation of the oscillator 3 may be interrupted.

The sequential switching operations of the switching MISFET Q_1 to Q_4 of the step down circuit 1 are interrupted by the interruption of the operation of the oscillator 3 so that the voltage on the line l_2 is further reduced. In the complementary type MISFET circuit constituting the level shifting circuit 12, as shown in Figure 6, if the complementary inverter circuit comprising the MISFETs Q_{24} and Q_{25} is rendered substantially nonconductive by the reduction in the voltage V_{CL} whilst the MISFET Q_{22} is conductive, the following undesired circuit operations occur.

When the voltage V_{CL} is dropped, the n-channel type MISFET Q_{24} is not rendered conductive even if the input voltage V_I is raised to the high level such as zero volts or earth potential. As a result the MISFET Q_{24} is left non-conductive, and the MISFTET Q_{23} cannot be rendered conductive.

Consequently, in the circuit shown in Figure 1, if the output voltage V_{CL} of the voltage regulator 2 is reduced to a lower level than the operating lower limit voltage of the complementary inverter by a drop in the voltage on the line l_2, the level shifting circuit 12 ceases to generate the clock pulses at a level which can simultaneously render the switching MISFETs Q_1 to Q_3 conductive.

As a result, in the case where only the latch circuit is provided for the purpose of the starting operation, in order to re-start the oscillations from the state at which the oscillations ceased, it becomes necessary to restore the starting latch circuit to its initial state by a process of once removing the battery voltage source and to release the latch operation with the MISFETs Q_{22} and Q_{20} of the level shifting circuit 12.

It is possible to prevent the voltage V_{CL} from being reduced to the undesired level by the provision of an oscillation detector 10 after the voltage supply has been connected. As a result, the operation of the oscillator 3, which has ceased to operate for the reason given above, is restarted.

The oscillation detector 10 comprises: inverters IV_2 to IV_6, which are operated by the supply voltage V_{CL} on the line l_3; an exclusive OR circuit EOR; resistors R_4 and R_5; and capacitors C_{12} and C_{13}.

The oscillation detector 10 is supplied with a predetermined output of the frequency divider 5, e.g., the inverted output $\overline{Q}$ of the flip-flop circuit FF_5 of Figure 4.

The operation of the oscillation detector 10 will now be described with reference to the waveforms shown in Figure 3.

At a time t_0, the battery voltage supply V_{SS} is connected. Since the exclusive OR circuit EOR has its two input terminal receiving the signals at such a high level as is substantially equal to earth potential, it generates a signal at a low level substantially equal to the supply voltage V_{CL}, as indicated by a waveform C in Figure 3. The MISFET Q_{17} is rendered non-conductive by the low level output signal of the exclusive OR circuit EOR. The signal at the input terminal of the inverter IV_5 acting as a waveform shaping circuit has its level raised to a high level by the capacitor C_{13} which is substantially equal to earth potential, as indicated by a waveform E in Figure 3. The output signal of the inverter IV_6 is correspondingly raised to the high level as indicated by a waveform F in Fig. 3.

In accordance with the oscillation starting characteristics of the quartz crystal unit X_{tal}, the reference frequency signal starts to be supplied from the oscillator 3 at a time t_1, as indicated by a waveform A in Fig. 3.

As a result that the amplitude of the output reference frequency signal of the oscillator 3 is made sufficiently large at a time t_2, the frequency divider 5 starts to respond to the reference pulse signal which is supplied through the waveform shaping circuit 6.

As a result that a predetermined number of reference pulse signals are applied after the time t_2, a signal, which is made to have the low level at a time t_3, as indicated by a waveform B in Fig. 3, is supplied from the frequency divider 5 to a line l_8.

The exclusive OR circuit EOR is supplied with an input signal which becomes incoincident for such a delay period as is determined by a delay circuit including the inverters IV_2 and IV_3, the resistor R_4 and the capacitor C_{12}. As a result, the exclusive OR circuit EOR generates a signal which has the high level for a period corresponding to the delay time period.

By means of the high level signal of the exclusive OR circuit EOR, a MISFET Q_{17} is rendered conductive so that the output signal of the inverter IV_4 is made to have the low level. As a result, the capacitor C_{13} is supplied with the low level signal of the inverter IV_4 through the MISFET Q_{17}. This MISFET Q_{17} is rendered non-conductive in accordance with the fact that the output signal of the exclusive OR circuit EOR is made to restore the low level. As a result, the low level signal is held in the capacitor C_{13}. Likewise, each time the signal level to be supplied from the frequency divider 5 to a line l_8 at and after a time t_4, the capacitor C_{13} is supplied with the low level signal. As a result, a signal is generated on a line l_{21} which is shown by a waveform E in Fig. 3.

In a manner to correspond to the low level signal on the line l_{21}, a low level signal as indicated by a waveform F in Fig. 3 is supplied by the inverter IV_6 to a line l_{22}.

The low level signal supplied by the inverter IV_6

is the oscillatory operation detecting signal of the oscillator 3.

In order that the oscillatory operation detecting signal may be changed from the low to high level before the output voltage V_{CL} of the voltage regulator 2 has dropped to the operating lower limit voltage of the circuit, such as the clock generator 11 or the level shifting circuit 12, as a result of the oscillation interruption of the oscillator 3, the resistor R_5 is connected in parallel with the capacitor C_{13}.

As a result, if the oscillating operation of the oscillator 3 is interrupted as in the case immediately after the starting state has ended, the step down circuit 1 is made to automatically restore the starting state.

The frequency divider 5 and the clock generator 11 are shown in detail in Fig. 4.

The clock generator 11 comprises latch circuits LA_1 to LA_4, NAND circuits ND_1 to ND_7 and an inverter IV_8. Each of the latch circuits LA_1 to LA_4 consists of two NOR circuits. The latch circuits LA_1 and LA_2, the NAND circuit ND_1 and the inverter IV_8 together constitute a start control circuit.

By means of the latch circuit LA_1, the high level signal on the line l_9 is deemed as a set signal, and the high level signal on a line l_{10} is deemed as a reset signal. Likewise, by means of the latch circuit LA_2, the high level signal on a line l_{23} is deemed as a set signal, and the high level signal on the line l_{22} is deemed as a reset signal.

When the battery voltage supply V_{SS} is connected, the respective flip-flops FF1 to FF16 constituting the frequency divider 5 are respectively reset by the high level signal which is supplied through the line l_{12} from the time adjusting circuit 13.

The latch circuit LA_1 is set by the high level signal, as indicated by a waveform B in Fig. 3, which is supplied through the line l_9 from the flip-flop FF5.

The latch circuit LA_2 is reset by the high level signal, as indicated by a waveform F in Fig. 3, which is supplied through the line l_{22} from the oscillation detector 10. As a result, the signal, which is supplied from the latch circuit LA_2 to a line l_{24}, has the low level at the time t_0, as indicated by a waveform H in Fig. 3.

When the signal on the line l_{22} has the low level in response to the oscillation detection by the oscillation detector 10 at the time t_3, as indicated at the waveform F in Fig. 3, the latch circuit LA_2 is released from its reset state. As a result, the set signal is not supplied to the line l_{23} at the time t_3, and the signal on the line l_{24} is held at the low level, as indicated by the waveform H in Fig. 3.

At a time t_5 one second after the frequency divider 5 has started its frequency dividing operation, the non-inverting output of the flip-flop FF16 is changed from the low level to the high level, as indicated by the waveform C in Fig. 3. The latch circuit LA_1 is correspondingly reset.

A NAND circuit ND_1 has its two input terminals receiving such signal as are simultaneously made to have the high level only for the delay period of a NOR circuit NR_2 of the latch circuit LA_1.

The result is that the high level signal indicated by a waveform G in Fig. 3 is supplied to the line l_{23} through an inverter IV_8 from the output of the NAND circuit ND_1.

The latch circuit LA_2 is set by the high level signal on the line l_{23} so that the high level signal as indicated by the waveform H in Fig. 3 is supplied to the line l_{24}.

The low level signal on the line l_{24} is deemed as a starting state indicating signal.

The clock pulses ϕ_1' to ϕ_3' output from NAND circuits ND_5 to ND_7, respectively, simultaneously have the high level in accordance with the starting state indicating signal.

The clock pulses ϕ_1' to ϕ_3' are supplied through the level shifting circuit 12 to the switching MISFETs Q_1 to Q_4 of the step down circuit 1.

When steady operation is indicated by the fact that the signal on the line l_{24} has the high level, the clock pulses ϕ_1' to ϕ_3' are changed in the following manner.

The output signals at the non-inverting output terminals of the flip-flops FF3 to FF5 of the frequency divider 5 are illustrated by waveforms A to C in Fig. 5.

The NAND circuit ND5 generates by means of the connections shown in Fig. 4, the clock signal in phase with the output signal of the flip-flop FF5, as indicated by a waveform G in Fig. 5.

A latch circuit LA_3 generates such a signal as is indicated by a waveform D in Fig. 5 in response to both the non-inverting output signal of the flip-flop FF3 and the inverted output signal of the flip-flop circuit FF5.

A NAND circuit ND_2 generates such a signal as is indicated by the waveform F in Fig. 5 upon reception of the non-inverting output signals of the flip-flop circuits FF3 and FF4.

A NAND circuit ND_3 is supplied with the output signals of the latch circuit LA_3 and the NAND circuit ND_2, and the NAND circuit ND_6 is supplied with the output signal of the NAND circuit ND_3 so that such a clock signal ϕ_2' as is indicated by a waveform H in Fig. 5 is output from the NAND circuit ND_6.

Likewise, a latch circuit LA_4 generates a signal as is indicated by waveform E in Fig. 5 upon reception of the non-inverting output signals of the flip-flop circuits FF3 and FF5.

The NAND circuit ND_7 generates a clock signal ϕ_3' as is indicated by a waveform I in Fig. 5 in response to the output signals of the latch circuit LA_4 and the NAND circuit ND_2.

By means of the clock signal ϕ_1' of Fig. 5, the switching MISFET Q_3 of the step down circuit 1 of Fig. 1 is rendered conductive during the period of t_{10} to t_{13} of one period t_{10} to t_{18} of the clock signal.

The switching MISFET Q_1 is rendered conductive from the time after the time period Z_1 has elapsed from the time t_{10} and is rendered non-conductive at the time t_{12} which is earlier by the time period Z_2 than the time t_{13}.

The switching MISFET Q_4 is rendered conductive for the time period from the time t_{13} to the time t_{16}.

The switching MISFET Q_2 is rendered conductive from the time after the time period Z_3 has elapsed from the time t_{13} and is rendered non-conductive at the time t_{15} which is earlier by the time period Z_4 than the time t_{16}.

Accordingly, the undesired rise in the output voltage of the step down circuit 1 can be prevented.

As is well known in the art, the capacitance of a battery is determined by the product of the discharging current (or output current) of the battery and the time period. For the identical capacitance, a battery having a larger electromotive force will have a larger storage energy. The electromotive force of the silver oxide battery is about 1.5 V, whereas the lithium battery has an electromotive force of about 3 V. Therefore, the lithium battery has a storage energy per unit volume about twice as large as that of the silver oxide battery.

In the case of the alternative form, where the step down circuit 1 is omitted, the voltage regulator 2 is directly supplied with the voltage of the battery power supply V_{SS}. In this case, by the use of the voltage regulator 2, such currents based upon both the through current and the charging and discharging currents to and from the capacitors as are to be consumed by the respective circuits to receive the output voltage of the voltage regulator 2 can be reduced. However, a current substantially equal to that which flows through the voltage regulator 2 will flow through the battery so that the characteristics of the lithium battery having a high storage energy cannot be sufficiently utilized.

By means of the step down circuit 1 and the voltage regulator 2, the current to be supplied from the lithium battery can be reduced to I/2 if the current which flows from the voltage regulator 2 to the electronic circuit is indicated by I. Moreover, the voltage to be applied to the voltage regulator 2 can be reduced to one half of the battery voltage V_{SS}. As a result, the power loss at the voltage regulator 2 can be reduced. On the other hand, the respective electronic circuits are operated under a low voltage in the vicinity of the operating lower limit voltage by the voltage regulator 2. As a result, the power consumptions of the respective electronic circuits can be reduced.

By using a lithium battery, it is possible to provide an electronic watch having a low power consumption and thus increase the life of the battery more than that in cases where a silver oxide battery is used as the battery.

Moreover, since the predetermined switching MISFETs of the step down circuit 1 are simultaneously rendered conductive at the starting state, special switching MISFETs are unnecessary.

Furthermore, the step down circuit 1 contains no circuit elements which have a relatively large size and complex construction e.g., an inductor. Therefore, the step down circuit 1 is suitable in such a device, e.g., an electronic wrist watch which is required to be of small size.

A second embodiment is shown in Fig. 10. A capacitor C_3 having a relatively large capacitance is connected to the output terminal of the voltage regulator 2 through an external terminal P_{11}. The other circuits which are shown in Fig. 10 have the same construction as those of the first embodiment shown in Fig. 1.

The capacitor C_3 is provided by the following reasons.

In the voltage regulator shown in Fig. 10 the control MISFET Q_{14} has a relatively small current flow therethrough so that it has a relatively high impedance. On the other hand, the signals to be generated at the respective nodes of the level shifting circuit 22 and the differential amplifier 20 both constituting the voltage regulator 2 are changed at relatively low rates partly because those circuits 22 and 20 are operated by the small currents, respectively, and partly because capacitances such as parasitic capacitances exist at or are coupled to the respective circuit modes.

On the other hand, a consumption current as is determined by the through current and by the charging and discharging currents to and from the capacitance flows through the frequency divider 5, the waveform shaping circuit 6. That current to be consumed by the circuits 5 and 6 is relatively quickly changed in a periodical manner in accordance with the operating states of the circuits 5 and 6.

As has been described above, the voltage regulator 2 has a relatively low operating rate and a relatively high output impedance so that the voltage on the line l_3 is relatively quickly changed in accordance with the operating states of the circuits 5 and 6. The fluctuations in the voltage on the line l_3 cause an undesired interference amongst the respective circuits which are coupled to the line l_3.

If the capacitor C_3 is provided, the impedance of the line l_3 can be sufficiently reduced so that the undesired interference can be prevented.

A third embodiment is shown in Fig. 11. In this embodiment the stabilized power supply circuit can reduce the output impedance without increasing the external terminals and the capacitors of the IC. In this third embodiment, the construction of the circuits other than the step down circuit 1 and the voltage regulator 2 is identical to the two previous embodiments shown in Figs. 1 and 10. Accordingly, an explanation of the circuits other than the circuits 1 and 2 will be omitted.

In the third embodiment, the step down circuit 1 and the voltage regulator 2 are integrated, as will be apparent from the following description. Specifically, the capacitor C_3, which corresponds to the capacitor C_2 connected to earth is connected with the output terminal of the control MISFET Q_{14}, which forms part of the voltage

regulator 2, through the external terminal P_{11}. In other words, the circuit of this third embodiment is equivalent to that which could be constructed by eliminating the capacitor C_2 and the terminal P_5 from the circuit of the second embodiment shown in Fig. 10.

The operations of the circuit according to the third embodiment will now be described in detail with reference to the circuit diagrams shown in Figs. 12A and 12B which illustrate the operating principles thereof.

Fig. 12A illustrates the state, at which the MISFETs Q_1 and Q_3 are rendered conductive. The switches SW_1 and SW_2 are connected to their E and H contacts, respectively. The capacitors C_4 and C_3 are connected in series through the control MISFET Q_{14} so that they are charged by the battery voltage supply V_{SS}. In this charging operation, the control MISFET Q_{14} is rendered substantially non-conductive by the output of the differential amplifier 20 when the charging voltage of the capacitor C_3 reaches the reference voltage. As a result the capacitors C_1 and C_3 are charged with substantially equal charges.

On the other hand, Fig. 12B illustrates the state, at which the MISFETs Q_2 and Q_4 are rendered conductive. The switches SW_1 and SW_2 are connected to their F and G contacts, respectively, so that the capacitor C_1 is disconnected from the battery voltage supply V_{SS}. At this particular state, the capacitors C_1 and C_2 are connected in an identical polarity substantially in parallel with each other through the MISFET Q_{14}. In this parallel connection, the capacitor C_1 is connected in parallel with the capacitor C_3 through the MISET Q_{14} so that the charging voltage of the capacitor C_3 is maintained at a constant voltage irrespective of the current consumption of the electronic circuit.

Since the capacitor C_3 is connected to the output terminal of the voltage regulator 2, the output impedance of the power supply circuit can be sufficiently reduced, and the fluctuations in the constant output voltage can be reduced to a low level similar to the circuit of the embodiment shown in Fig. 10. Moreover, since only the two external capacitors are sufficient for the IC, the circuit of the third embodiment is very useful especially in the case where it is applied to a device having limited mounting space e.g., a thin type electronic wrist watch.

In the circuit shown in Fig. 11, it is preferred for the following reason that the capacitor C_1 has a smaller capacitance than the capacitor C_2.

The timing pulses $\emptyset_1$ to $\emptyset_3$ have the high level similar to the circuits shown in Figs. 1 and 10 by the high level of the oscillatory detecting signal, which is supplied at the start to the line l_{22}, so that the MISFETs Q_1, Q_2 and Q_3 are simultaneously rendered conductive by the timing pulses $\emptyset_1$ to $\emptyset_3$ at that high level whereas the MISFET Q_4 is rendered non-conductive. As a result, the battery voltage V_{SS} is applied directly to the voltage regulator 2 so that the capacitor C_3 is charged at a predetermined constant voltage. At this time, the capacitor C_1 is not charged because the MISFET Q_2 is rendered non-conductive, as has been described above. As a result of the fact that the capacitor C_1 is not charged during the starting operation as in the above, the circuit performs the following undesired operation only during a predetermined time period after the start has ended. Waveforms A to E in Fig. 13, respectively illustrate the signal at the line l_{24} (which is shown in Fig. 4) in the clock generator when the battery voltage supply is connected at the time t_0 and when the starting state is ended at the time t_8, the clock pulses $\emptyset_1$ to $\emptyset_3$, and the output voltage of the voltage regulator 2.

First of all, by raising the signal on the line l_{24} to the high level at the time t_5, the clock pulses $\emptyset_2$ and $\emptyset_3$ of the clock pulses $\emptyset_1$ to $\emptyset_3$ have the low level, as indicated by the waveforms C and D in Fig. 13. As a result, the switching MISFETs Q_1, Q_2 and Q_4 are rendered non-conductive, whereas the switching MISFET Q_3 is rendered conductive.

Next, when the clock pulse $\emptyset_2$ has the high level at a time t_6, as indicated by the waveform C, the line l_2 is supplied with the voltage of the battery voltage supply V_{SS} through the MISFET Q_1, the capacitor C_1 having at that instant zero capacitance, and the MISFET Q_3. In this case, since the capacitor C_3 is charged in advance during the starting operation, no more than a relatively small charging current flows through the capacitor C_1. Therefore, the voltage across the capacitor C_1 can be deemed to be substantially zero.

As a result of the fact that the clock pulse $\emptyset_2$ has the low level at a time t_7, the MISFET Q_1 is rendered non-conductive.

If the MISFET Q_4 is rendered conductive as a result of the fact that the clock pulse $\emptyset_1$ has the low level at a time t_8, the source of the MISFET Q_2 falls substantially to earth potential through the MISFET Q_4 and the capacitor C_1 which at that instant has substantially zero capacitance. At this time, the MISFET Q_2 has its drain D supplied with the output voltage of the capacitor C_3 through the control MISFET Q_{14} and the line l_2 so that the pn junction (i.e., the drain junction) between its drain D and a substrate gate SUB is biased in the forward direction. As a result, the charges stored in the capacitor C_3 are distributed to the capacitor C_1 through the drain junction between the control MISFET Q_{14} and the switching MISFET Q_2. In other words, the voltage supplied to the line l_3 starts to have even its absolute value reduced, as indicated by the waveform E in Fig. 13.

If the clock pulse $\emptyset_3$ has the high level at a time t_9, the MISFET Q_2 is rendered conductive as a result that the p-type well region (although not shown) below its gate electrode is formed on its surface with a channel region. As a result, the charging voltage of the capacitor C_3, i.e., the voltage on the line l_3 is further reduced, as indicated by the waveform E in Fig. 13.

If clock pulse $\emptyset_2$ again has the high level at the time t_{10}, the line l_2 is supplied with the voltage of the battery voltage supply V_{SS} similar to the

circuit operation at the time t_6 through the MISFET Q_1, the capacitor C_1 having been charged by the charge distribution, and the MISFET Q_3 so that the charging voltage of the capacitor C_3 is again raised, as indicated by the waveform E in Fig. 13, to the level which is determined by the characteristics of the voltage regulator 2.

The fluctuations in the charging voltage of the capacitor C_3 are reduced, as indicated by the waveform E in Fig. 13, by repeating the switching operations of the MISFET Q_1 to Q_4 because the charges of the capacitor C_1 are gradually increased.

When the voltage on the line l_3 is reduced, the oscillator 3 stops. If the voltage drop on the line l_3 is substantial, a problem arises in that the step down circuit cannot again be brought into its starting state.

In the third embodiment shown in Fig. 11, the capacitor C_1 does not have a capacitance equal to that of the capacitor C_3 but has a smaller capacitance than that of the capacitor C_3. As a result, the charges to be distributed from the capacitor C_3 to the capacitor C_1 immediately after the start has ended can be reduced so that the voltage drop across the capacitor C_3 can be reduced.

In the case where the capacitance of the capacitor C_1 is made smaller than that of the capacitor C_3, the following advantage results. In the normal operation after the charge distribution from the capacitor C_3 to the capacitor C_1 has ceased, the capacitor has a relatively large charging voltage as a result of the fact that its capacitance is small. If the charging voltage of the capacitor C_1 thus has a large value, it can be distributed at a relatively high rate to the capacitor C_3 when the MISFETs Q_2 and Q_4 are rendered conductive. As a result, in the case where the voltage across the capacitor C_3 is reduced, it can restore the voltage thereacross to a desired value at a relatively high rate. Incidentally, the capacitor C_3 is desired to be charged to the stabilised output voltage V_{CL} when it is connected in series with the capacitor C_1. It is, therefore, desired that the capacitance ratio between the capacitors C_1 and C_2 be restricted to such a value as corresponds to the ratio between the voltage V_{CL} desired and the battery voltage V_{SS}.

In order to prevent those fluctuations in the output voltage V_{CL} which result from the fact that the capacitor C_1 is not charged in advance, it is conceivable that the capacitor C_1 is charged at the starting state. For this purpose, the internal construction of the clock generator 11 may be suitably modified such that the clock pulse ϕ_1 has the high level whereas the clock pulses ϕ_2 and ϕ_3 have the high level at the starting state. However, even if the capacitor C_1 is thus charged in advance, it is difficult for the following reason to eliminate the fluctuations in the charging voltage of the capacitor C_3 after the starting state has ended.

In the case where the modification is made, the capacitor C_1 is charged at the starting state substantially to the voltage of the battery voltage supply V_{SS}. Thus, if the MISFETs Q_1 and Q_3 are rendered conductive after the starting state has been ended, the line l_1 is supplied with the voltage at such a level, i.e., at a zero level as is determined by subtracting the charging voltage of the capacitor C_1 from the output voltage of the battery voltage supply V_{SS}. As a result, the voltage of the capacitor C_3, i.e., the voltage on the line l_3 fluctuates by the circuit operation.

A fourth embodiment is shown in Fig. 14. In this fourth embodiment, it is considered that the impedance at the output terminal of the voltage regulator 2 is sufficiently reduced by the capacitor C_3 which is coupled to the IC through the external terminal P_{11} and that the two capacitors coupled to the IC may be identical to each other.

As a result, the assembling of the electronic watch can be facilitated.

A MISFET Q_{30} is connected between the common node between the switching MISFETs Q_1 and Q_2 and the terminal P_3, and a MISFET Q_{31} is connected between the external terminal P_3 and the line l_3.

The MISFET Q_{31} has its gate supplied with a waveform A shown in Fig. 15, with a start control signal A which has an amplitude of $-V_{SS}$ and which has the low level (i.e., $-V_{SS}$) when the starting state of the power supply is ended. That start control signal A can be prepared by applying the signal, which is supplied to the line l_{24} of the circuit of Fig. 4, to the level shifting circuit shown in Fig. 6.

The MISFET Q_{30} has its gate supplied with the start control signal A through an inverter IN which is operated directly by the battery voltage supply V_{SS}.

The signals, which have their levels shifted to the voltage level V_{SS} and which have opposite phases to each other so that they may be supplied to the gates of the MISFETs Q_{30} and Q_{31}, may be generated from the drains of the MISFETs Q_{20} and Q_{22} of the level shifting circuit shown in Fig. 6. If this modification is made, the inverter IN can be omitted.

The clock pulse ϕ_1 at the starting state is made to have the low level, whereas the clock pulses ϕ_2 and ϕ_3 are made to have the high level.

In order to obtain the clock pulse ϕ_1, the NAND circuit ND_5 of Fig. 4 is replaced by a NOR circuit, which is supplied with both the inverted output signal of the flip-flop circuit FF5 and such a signal as is prepared by inverting the signal on the line l_{24} by means of an inverter.

The operation of the fourth embodiment shown in Fig. 14, will now be described.

First of all, as indicated by the waveform A in Fig. 15, as a result of the fact that the start control signal A is at the high level during the starting time period from the time t_0 to the time t_5, the MISFET Q_{31} is rendered conductive, whereas the MISET Q_{30} is rendered non-conductive.

During that starting time period, as a result that the clock pulse ϕ_1 has the low level whereas the

clock pulses ϕ_2 and ϕ_3 have the high level, as has been described hereinbefore, the switching MISFETs Q_1, Q_2 and Q_4 are rendered conductive, whereas the switching MISFET Q_3 is rendered non-conductive.

As a result, the line l_2 is supplied with the voltage of the battery power supply V_{SS} through the switching MISFET Q_1 and Q_2 which are conductive. As a result of the fact that the MISFETs Q_{31} and Q_4 are conductive at that time, the capacitor C_1 is connected in parallel with the capacitor C_3 through the MISFETs Q_{31} and Q_4. Incidentally, as a result of the fact that the MISFET Q_{30} is non-conductive, a direct current path is not established between the capacitor C_1 and the battery voltage supply V_{SS}.

As a result, both the capacitors C_1 and C_3 are charged to the voltage which is determined by the voltage regulator 2.

As a result of the fact that the start control signal A has the low level at the time t_5, the starting state is ended. After this end, the MISFET Q_{30} is rendered conductive whereas the MISFET Q_{31} is rendered non-conductive.

As has been described above, the capacitor C_1 is charged to the voltage V_{CL} at the starting state. As a result, after the starting state has ended, the charge distribution from the capacitor C_3 to the capacitor C_1 does not take place so that the voltage across the capacitor C_3, i.e., the voltage at the line l_3 can be made constant, as indicated by a waveform F in Fig. 15, notwithstanding whether it is at the starting state or not.

Incidentally, the voltage at the line l_2, which is connected to the drain of the control MISFET Q_{14} of the voltage regulator 2, is so changed during the normal operation after the starting state has ended, as is indicated by a waveform E in Fig. 15.

The voltage on the line l_2 has a value, which is determined by subtracting the charging voltage of the capacitor C_1 from the voltage of the battery voltage supply V_{SS}, as a result of the fact that the switching MISFETs Q_1 and Q_3 are rendered conductive at the time t_6. The charging operations of the capacitors C_1 and C_3 at that time substantially cease when the voltage at the line l_3, i.e., across the capacitor C_3 has the level which is determined by the voltage regulator 2. The charging voltage of the capacitor C_1 is accordingly reduced to a relatively small value so that the voltage on the line l_2 has a relatively large value.

On the contrary, as a result of the fact that the switching MISFETs Q_4 and Q_2 are rendered conductive at the time t_9, the charging voltage of the capacitor C_1 is supplied to the line l_2. As a result, the voltage on the line l_2 falls to a relatively small value, as shown in waveform E.

A fifth embodiment is shown in Fig. 16. In order to make it possible to use a battery for a relatively long period, i.e., in order to increase the life of the battery, a stabilized output voltage having a sufficient value can be generated by the voltage regulator 2 even if the voltage of the battery voltage supply V_{SS} falls to a relatively low level.

In the fifth embodiment, although the step down circuit 1 and the voltage regulator 2 are integrated with each other, they are assumed to be made separate for the sake of convenience in the following description. In this the voltage to be supplied from the step down circuit 1 to the line l_2 is made to have about one half of the voltage of the battery voltage supply V_{SS}. Consequently, the relationship between the voltage of the battery voltage supply V_{SS} and the voltage on the line l_2 is illustrated by the characteristic curve l_2 in the graphical presentation of Fig. 17.

Since the voltage regulator 2 receives the output voltage of the step down circuit 1, it generates the stabilized voltage V_{CL} if the output voltage of the step down circuit 1 is substantially equal to or higher than the stabilized voltage V_{CL}.

If, in the case where the voltage regulator 2 is supplied exclusively with the step down voltage which is generated by the step down circuit 1, the step down voltage is reduced to a lower level than the stabilised voltage V_{CL} by a slight reduction in the voltage of the battery voltage supply V_{SS}, the output voltage of the voltage regulator 2 is accordingly reduced. The output voltage of the voltage regulator 2 is reduced from the point D in Fig. 17 generally along the characteristic curve l_2. As a result, notwithstanding that a relatively high voltage is being generated by the battery power supply V_{SS}, it becomes necessary to replace the battery voltage supply.

In order to operate the circuit at all times even when the battery voltage is relatively reduced, in other words, in order to prolong the life of the battery, the voltage of the battery power supply V_{SS} is supplied directly to the voltage regulator 2 when the battery voltage has such a level as to reduce the step down voltage substantially to the stabilized voltage V_{CL}. Then, the output voltage of the voltage regulator 2 is stabilized until the voltage of the battery voltage supply V_{SS} is reduced to a level indicated at a point C in Fig. 17, namely, until the voltage of the battery voltage supply V_{SS} falls to a level V_{SS}'' which is substantially equal to the stabilized voltage V_{CL}.

The operation of the fifth embodiment shown in Fig. 16 will now be described in detail.

The step down circuit 1 has a construction similar to that of the circuit of Fig. 14. At the starting state, the clock pulse ϕ_1 has the low level, whereas the clock pulses ϕ_2 and ϕ_3 have the high level. The switching MISFETs Q_1, Q_2 and Q_4 are accordingly rendered conductive, whereas the switching MISFET Q_3 is rendered non-conductive. On the other hand, the MISFET Q_{30} is rendered non-conductive in response to a control signal $\overline{A}$ at the low level as is supplied from a level shifting circuit 29, whereas the MISFET Q_{31} is rendered conductive by the control signal A at the high level.

The voltage regulator 2 is constructed similarly to the respective embodiments of the control MISFET Q_{14}, the differential amplifier 20, the

reference voltage generator 21 and the level shifting circuit 22.

A clock circuit 31 is formed with a plurality of power supply wirings and is additionally formed with a level shifting circuit, if necessary. The clock circuit 31 is basically constructed of a variety of known circuits, for example, of: an oscillator for generating a reference frequency signal; a frequency divider which receives the reference frequency signal from the oscillator in order to generate a second clock signal; a variety of time counters which receive the output signal of the frequency divider in order to generate time data such as ten seconds, one minute, ten minutes, one hour, ten hours, one day or ten days; a display decoder for converting the output signals of the various time counters into display signals; an output buffer circuit which receives the output signal of the display decoder; a stop watch circuit; an alarm circuit; a mode selector which detects the operation order of the switches SW_1 and SW_2, which are connected between the external terminals P_{10} and P_{22} and earth, in order to select a variety of modes of the watch such as a normal watch operation mode, a time correcting mode, a stop watch mode or an alarm mode; a control circuit for controlling the operations of the various circuits in accordance with the combinations of the output signal of the mode selector and the signal from the switch SW_1 or SW_2; and an output buffer circuit which receives the output signal of the alarm circuit (although all of the circuits are not shown).

On the other hand, the watch circuit 31 may also be constructed of a well-known ROM-RAM type circuit which includes: an oscillator; a timing pulse generator; a random access memory for writing time data, operation mode data, stop watch data or alarm data; a read only memory (or ROM) for writing micro-instruction; a program counter; an arithmetic logical unit; and a variety of decoders.

From the watch circuit 31 thus constructed, there are generated: a display decode signal for driving a display DSP having liquid crystal segments, which are arranged in the form of a squarish numeral "8" for each figure, as shown; a signal for driving acoustic converting means SP which is provided to generate an alarm sound and which is constructed of a piezoelectric element; and a variety of clock and control signals to be supplied to a variety of such circuits as will be described in the following.

The output buffer circuit, which is arranged in the clock circuit 31 in order to drive the acoustic converting means SP, requires such a relatively large drive current that it is operated by the direct voltage of the battery, voltage supply V_{SS}.

A comparator 25 is provided in order to detect the voltage of the battery voltage supply V_{SS}. This comparator 25 has its non-inverting input terminal supplied with the reference voltage, which is generated by the reference voltage generator 21, and its inverting input terminal supplied with the voltage of the battery voltage supply V_{SS} through a voltage divider which comprises resistors R_2 and R_3.

The divided voltage supplied by the voltage divider (R_2 and R_3) is made equal to the output voltage of the reference voltage circuit 21 by suitably setting the voltage dividing ratio of the resistors R_2 and R_3 when the voltage of the battery voltage supply V_{SS} falls to a level to be detected (i.e., a detection level), i.e., to a level equal to or slightly higher than the value V_{SS}' indicated in Fig. 17.

As a result, when the voltage of the battery voltage supply V_{SS} falls to a level equal to or lower than the detection level, the output voltage of the comparator 25 is accordingly raised to the high level.

The voltage divider (R_2 and R_3) and the comparator 25 are intermittently operated so as to reduce their respective average currents to be consumed. In order to intermittently operate the voltage divider (R_2 and R_3), there is provided a switching MISFET Q_{32} which is rendered conductive by a clock pulse ϕ_0. On the other hand, the comparator 25 is supplied with the same clock pulse as the clock pulse ϕ_0 to be supplied to the switching MISFET Q_{32}.

Incidentally, the comparator 25 has a construction similar to that of the differential amplifier 20 shown in Fig. 1. For the sake of the intermittent operations, the MISFET similar to the constant current MISFET Q_{13} of Fig. 1 has its gate supplied with the clock pulse ϕ_0.

A latch circuit 26 is provided so as to generate a series of signals on the basis of the intermittent output signals which are supplied to the comparator 25.

Since the comparator 25 is rendered operative by the clock pulse ϕ_0, the latch circuit 26 has its data input terminal $\overline{CL}$ supplied with the same clock pulse as the clock pulse ϕ_0 which is supplied to the comparator 25.

The clock pulse ϕ_0 can be supplied by waveform shaping circuit 30 which receives reference clock signals having respective frequencies as are generated by the clock circuit 31, as shown. Incidentally, by generating the clock pulse ϕ_0 from the circuit having the construction described above, the changing timing of the output signal of the latch circuit 26 and the changing timing of the clock pulses ϕ_1 to ϕ_3 can be synchronized.

The output signal of the latch circuit 26 is supplied through a NOR gate 27 to a start control circuit 28.

Incidentally, the gate circuit 27 is provided to correspond to the fact that the electronic watch is equipped with such display means, e.g., the alarm circuit and the acoustic converting means SP to be driven by the output of the alarm circuit as requires a relatively large drive current, as has been described above.

The gate circuit 27 has its one input terminal supplied such a control signal ϕ_c through a line l_{41} from the control circuit in the clock circuit 31 as is raised to the high level in synchronism with the

timing at which the drive current flows through the display means DSP and SP.

In this case, the battery voltage supply V_{SS} usually has such a relatively large internal resistance that its output voltage is substantially reduced if a large current flows in accordance with the large drive current. This reduction in the voltage of the battery voltage supply V_{SS} is resultantly detected by the comparator 25. It should, however, be noted that a slight time delay occurs until the reduction of the voltage is detected.

In the case where the gate circuit 27 and the control signal $\emptyset_C$ are used, it becomes unnecessary to await the voltage drop detection output based upon the output signal of the comparator 25.

As will become apparent from the following description, the voltage of the battery voltage supply V_{SS} is supplied to the voltage regulator 2, before such a circuit operation is started as to reduce the voltage of the battery voltage source V_{SS}, so that the undesired voltage drop on the line l_3 can be prevented.

In Fig. 16, the start control circuit 28 is indicated independently of a clock generator 11' so as to facilitate its understanding.

The start control circuit 28 is shown in greater detail in Fig. 18, and is so constructed that a NAND circuit ND_{10} and an inverter IV_{20} are added to the start control circuit shown in Fig. 4.

The NAND circuit ND_{10} has one of its input terminals supplied with a signal through a line l_{43} from the NOR gate circuit 27 (as shown in Fig. 16) which is reduced to the low level when the reduction in the battery voltage supply voltage is detected and when the alarm display is made. As a result, the start control circuit 28 supplies the low level signal to the line l_{23} not only during the start period but also when the output of the NOR gate 27 has the low level.

Incidentally, a portion of the clock generator 11' is also shown in Fig. 18. The clock pulse $\emptyset_1'$ supplied from a NOR circuit NR_{10} falls to the low level in a manner to correspond to the fact that the signal on the line l_{24} has the low level.

The operation of the circuit shown in Fig. 16 is indicated by the waveforms A to G in Fig. 19. In Fig. 19, incidentally, letters V_{DD}(+) implies earth potential, whereas letters V_{SS}(—) implies the potential corresponding to the output potential of the battery power supply V_{SS}.

It should be noted that even if the step down voltage becomes equal to or lower than the stabilized output voltage V_{CL}, the stabilized output voltage V_{CL} at a predetermiend level is generated by the switching operations so that the battery voltage V_{SS} can be effectively used. As a result, the life of the battery can be prolonged. Above all, the lithium battery has such a high internal resistance, e.g., several hundreds ohms that a large voltage drop takes place in the operation mode of a large current consumption. The addition of such a function as has been described above becomes especially suitable in the case where a lithium battery is used.

In a modified form, forming the sixth embodiment, the circuits 1 and 2 of Figs. 14 and 16 may be replaced by the circuit shown in Fig. 20. In Fig. 20, incidentally, the elements corresponding to the respective elements of the foregoing embodiments are indicated by identical reference characters.

In the circuit of Fig. 20, at the starting state and upon reduction in the battery voltage supply voltage, the clock pulses $\emptyset_1$ to $\emptyset_3$ and the control signal A have the high level, whereas the control signal $\overline{A}$ has the low level. In accordance with the respective signals at the respective levels, the switching MISFETs Q_1 to Q_3 and the MISFET Q_{31} are rendered conductive, whereas the switching MISFET Q_4 and the MISFET Q_{30} are rendered non-conductive. As a result, the capacitor C_1 is substantially connected in series with the battery voltage supply V_{SS} and the capacitor C_3. As a result of the fact that the capacitors C_1 and C_3 are connected in series, the capacitor C_3 is charged not only from the control MISFET Q_{14} constituting a part of the voltage regulator 2 but also through the capacitor C_1. As a result, when the battery voltage supply is connected, the rise of the voltage to be supplied to the line l_3 can be accelerated. At the same time, the capacitor C_1 is charged within a relatively short time period.

After the starting state has ended, the control signals A and $\overline{A}$ have the low and high levels, respectively, whereas the clock pulses $\emptyset_1$ to $\emptyset_3$ are consecutively changed similarly to the foregoing embodiments.

The step down circuit 1 and the voltage regulator 2 of Figs. 14 and 16 can be further modified, to form a seventh embodiment as shown in Fig. 21.

In the circuit shown in Fig. 21, as a result of the fact that the clock pulses $\emptyset_1$ to $\emptyset_3$ have the low level whereas the control signal A has the high level at the starting state and upon a reduction of the battery voltage supply voltage, the switching MISFETs Q_1 to Q_3 are rendered non-conductive whereas the switching MISFET Q_4 and the MISFETs Q_{30} and Q_{31} are rendered conductive. As a result, the control MISFET Q_{14} has its drain supplied through the MISFET Q_{30} with the battery voltage. On the other hand, the capacitor C_1 is supplied through the MISFET Q_{31} with the constant voltage which is supplied to the line l_3.

When the starting state has ended, the control signal A has the low level whereas the clock pulses $\emptyset_1$ to $\emptyset_3$ are consecutively changed in similar manner to the foregoing embodiments.

The charging and discharging paths of the capacitor C_1 after the starting state has ended are constituted exclusively of the switching MISFETs Q_1 to Q_4. As a result, it is possible to prevent such voltage and power losses from being established as will take place in the case where the MISFET Q_{30} is connected in series with the charging and discharging paths of the capacitor C_1. Moreover, since the MISFETs Q_{30} and Q_{31} are operated in

phase, it becomes sufficient to generate the single control signal A.

In further modified forms (not illustrated), the timing pulses to be supplied to the respective step down circuits 1 may have two phases. Nevertheless, in the case where the starting operation is to be performed by the use of the switching means of those step down circuits or in the case where the step down operations are ceased by the use of those switching means, it is convenient to use three-phase timing pulses which can simultaneously render the MISFETs Q_1 and Q_2 conductive without any difficulty.

Furthermore, the circuit of Fig. 16, which makes it possible to use the battery to generate a reduced voltage, can be similarly applied to the circuits of Figs. 1, 10, 11 and 14. Furthermore, the differential amplifier 20 of the voltage regulator 2 may be clock-driven to further reduce the current consumption. In this modification, the gate control voltage of the MISFET Q_{14} is maintained by the capacitor C_4.

Furthermore, the above described embodiments can be widely used in such a small-sized electronic device, e.g. an analog electronic watch or digital electronic watch which is driven by a battery.

Claims

1. An electronic circuit including:

(a) a first node arranged to be supplied with a power supply voltage;

(b) a second node;

(c) a step down circuit including a plurality of capacitors and a plurality of switching elements for connecting said capacitors in series during a first time period and in parallel during a second time period, said step down circuit being responsive to the power supply voltage supplied to said first node in order to supply a step down voltage to said second node;

(d) a voltage detector for detecting that said power supply voltage has fallen to a predetermined value; and

(e) a controller responsive to the detection signal which is supplied by said voltage detector, for controlling the step down circuit.

2. An electronic circuit according to Claim 1, wherein said step down circuit includes: a first switching element connected between said first node and a third node and arranged to be periodically turned on; a first capacitor connected between said third node and a fourth node; a second switching element connected between said fourthnode and a reference potential point of said circuit and arranged to be turned on when said first switching element is not turned on; a third switching element connected between said fourth node and said second node and arranged to be turned on substantially simultaneously with said first switching element; a fourth switching element connected between said third node and said second node and arranged to be turned on substantially simultaneously with said second switching element; and a second capacitor arranged to be charged by the voltage which is supplied to said second node.

3. An electronic circuit according to Claim 2, wherein said controller is arranged to simultaneously turn on at least said first and fourth switching elements on the basis of the output signal of said voltage detector.

4. An electronic circuit according to Claim 2, further including a voltage regulator responsive to the voltage which is supplied to said second node, in order to supply a constant voltage to said second capacitor.

5. An electronic circuit according to Claim 4, wherein said voltage detector is arranged to detect the voltage at said first node when the voltage supplied to said second node becomes substantially equal to the constant output voltage of said voltage regulator.

6. An electronic circuit according to Claim 5, wherein said voltage detector is rendered operative by the voltage which is supplied to said second node.

7. An electronic circuit according to Claim 6, wherein said voltage detecting circuit is rendered intermittently operative.

8. An electronic circuit according to Claim 2, wherein said first to fourth switching elements comprise insulated gate field effect transistors.

9. An electronic circuit according to Claim 8: wherein said first, third and fourth switching elements comprise first conduction type insulated gate field effect transistors; and wherein said second switching element comprises a second conduction type insulated field effect transistor which is opposite to said first conduction type.

10. An electronic circuit including:

(a) a first node arranged to be supplied with a power supply voltage;

(b) a second node;

(c) a step down circuit including a plurality of capacitors and a plurality of switching elements for connecting said capacitors in series during a first time period and in parallel during a second time period, said step down circuit being responsive to the power supply voltage supplied to said first node in order to supply a step down voltage to said second node;

(d) a load circuit responsive to at least the voltage, which is supplied to said second node, as the power supply voltage; and

(e) a controller for supplying the voltage, which is supplied to said first node, directly to said second node in accordance with the operating state of said load circuit.

11. An electronic circuit according to Claim 10, wherein said step down circuit includes: a first switching element connected between said first node and said third node and adapted to be periodically turned on; a first capacitor connected between said third node and a fourth node; a second switching element connected between said fourth node and a reference potential point of said circuit and arranged to be turned on during a time period other than the "ON" time period of said first switching element; a third switching

element connected between said fourth node and said second node and arranged to be turned on during substantially the same time period as that of said first switching element; a fourth switching element connected between said third node and said second node and arranged to be turned on during substantially the same time period as that of said second switching element; and a second capacitor arranged to be charged in accordance with the voltage which is supplied to said second node.

12. An electronic circuit according to Claim 11, further including:

(f) a voltage detector for detecting that said power supply voltage has fallen to a predetermined value; and

(g) a controller responsive to the detection signal, which is supplied by said voltage detector, for controlling the step down circuit.

13. An electronic circuit according to Claim 12, wherein said load circuit comprises a clock circuit.

14. An electronic circuit including:

(a) a first node arranged to be supplied with a power supply voltage;

(b) a second node;

(c) a first switching element connected between said first node and a third node and arranged to be periodically turned on;

(d) a first capacitor connected between said third node and a fourth node;

(e) a second switching element connected between said fourth node and a reference potential point of said circuit and arranged to be turned on when said first switching element is not turned on;

(f) a third switching element connected between said fourth node and a fifth node and arranged to be turned on in synchronism with said first switching element;

(g) a fourth switching element connected between said third node and said fifth node and arranged to be turned on in synchronism with said second switching element;

(h) a voltage regulator for supplying a predetermined voltage to said second node in accordance with the voltage which is supplied to said fifth node; and

(i) a second capacitor connected between said second node and the reference potential point of said circuit.

15. An electronic circuit according to Claim 14, wherein said first capacitor has a smaller value of capacitance than that of said second capacitor.

16. An electronic circuit according to Claim 14: wherein said switching elements and said voltage regulator are formed in a single semiconductor integrated circuit; and wherein said first and second capacitors are connected to said integrated circuit.

17. An electronic circuit according to Claim 16: wherein said first, third and fourth switching elements comprise first conduction channel type insulated gate field effect transistors; and wherein said second switching element comprises a second conduction channel type insulated gate field effect transistor.

18. An electronic circuit including:

(a) a first node arranged to be supplied with a power supply voltage;

(b) a second node;

(c) a first switching element connected between said first node and a third node and arranged to be periodically turned on;

(d) a first capacitor having one terminal connected with said third node and its other terminal connected with a fourth node;

(e) a second switching element connected between said fourth node and a reference potential point of said circuit and arranged to be turned on when said first switching element is not turned on;

(f) a third switching element connected between said fourth node and a fifth node and arranged to be turned on in synchronism with said first switching element;

(g) a fourth switching element connected between said third node and said fifth node and arranged to be turned on in synchronism with said second switching element;

(h) a voltage regulator for supplying a predetermined voltage to said second node in accordance with the voltage which is supplied to said fifth node;

(i) a second capacitor connected between said second node and the reference potential point of said circuit; and

(j) a charging circuit for charging said first capacitor to a voltage during a predetermined time period after the power supply is connected which is substantially equal to the output voltage of said voltage regulator.

19. An electronic circuit according to Claim 18, wherein said charging circuit includes: a fifth switching element connected between said third node and one terminal of said first capacitor and arranged to be turned on, until a predetermined time period elapses after the power supply has been connected and to be thereafter turned off; and a sixth switching element connected between said one terminal of said first capacitor and said second node and arranged to be complementarily switched with respect to said fifth switching element.

20. An electronic circuit according to Claim 19: wherein said switching elements and said voltage regulator are formed in a single semiconductor integrated circuit; and wherein said first and second capacitors are connected to said semiconductor integrated circuit.

21. An electronic circuit according to Claim 20, wherein said first and third to sixth switching elements comprise first conduction channel type insulated gate field effect transistors; and wherein said second switching element comprises a second conduction channel type insulated gate field effect transistor.

22. An electronic circuit according to Claim 18, further including a third capacitor connected

between said fifth node and said reference potential point.

23. An electronic circuit including:

(a) a first node arranged to be supplied with a power supply voltage;

(b) a second node;

(c) a step down circuit including a plurality of capacitors and a plurality of switching elements for connecting said capacitors in series during a first time period and in parallel during a second time period, said step down circuit being responsive to the power supply voltage supplied to said first node in order to supply a step down voltage to said second node; and

(d) a clock generator arranged to be operated by the voltage, which is supplied to said second node, in order to supply clock pulses for switching said switching elements.

24. An electronic circuit according to Claim 23, wherein said step down circuit includes: a first switching element connected between said first node and a third node; a first capacitor connected between said third node and a fourth node; a second switching element connected between said fourth node and a reference potential point of said circuit; a third switching element connected between said fourth node and said second node; a fourth switching element connected between said third node and said second node; and a second capacitor arranged to be charged in accordance with the voltage which is supplied to said second node.

25. An electronic circuit according to Claim 24, wherein said clock generator operates to generate at least both a clock pulse for simultaneously turning on said first and third switching elements and a clock pulse for simultaneously turning on said second and fourth switching elements.

26. An electronic circuit according to Claim 23, further including a level shifting circuit responsive to the clock pulses, which are supplied from said clock generator, in order to supply a clock pulse at the level of said power supply voltage, which is supplied to said first node, and first to fourth switching elements being switched by the output signal of said level shifting circuit.

27. An electronic circuit according to Claim 24, further including a voltage generator responsive to the voltage, which is supplied to said second node, in order to supply a constant voltage.

28. An electronic circuit according to Claim 24, further including a voltage regulator responsive to the voltage, which is supplied to said second node, in order to supply a constant voltage which is to be supplied to said second capacitor.

29. An electronic circuit according to Claim 28, further including a clock circuit responsive to the output voltage of said voltage regulator as the power supply voltage, said clock generator being responsive to the clock pulse, which is supplied by said clock circuit, in order to produce said clock pulses for controlling said first to fourth switching elements.

30. An electronic circuit according to Claim 29, wherein said clock circuit includes an output buffer circuit responsive to the voltage, which is supplied to said first node, as the power supply voltage.

31. An electronic circuit according to Claim 29: wherein said first to fourth switching elements, said voltage regulator, said clock circuit and said clock generator are formed in to a complementary type insulated gate field effect semiconductor integrated circuit device; and wherein said first and second capacitors are connected to said complementary type insulated gate field effect semiconductor integrated circuit device.

32. An electronic circuit including:

(a) a first node arranged to be supplied with a power supply voltage;

(b) a second node;

(c) a first switching element connected between said first node and a third node;

(d) a first capacitor connected between said third node and a fourth node;

(e) a second switching element connected between said fourth node and a reference potential point of ssaid circuit;

(f) a third switching element connected between said fourth node and said second node;

(g) a fourth switching element connected between said third node and said second node;

(h) a second capacitor arranged to be charged in accordance with the voltage which is supplied to said second node;

(i) a clock generator made operative by the voltage, which is supplied from said second capacitor, to generate clock pulses partly for substantially simultaneously turning on said first and third switching elements and partly for substantially turning on said second and fourth switching element during the time period which is different from the "ON" time period of said first and third switching elements, and

(j) a starter for supplying the voltage, which is supplied to said first node, to said fourth node during a predetermined time period when the power supply is connected.

33. An electronic circuit according to Claim 32, wherein said starter is made operative to supply signals for simultaneously turning on at least said first and fourth switching elements for said predetermined time period when said power supply is connected.

34. An electronic circuit according to Claim 32, further including an oscillator responsive to the voltage, which is supplied from said second capacitor, as the power supply voltage, said clock generator being responsive to the signal, which is generated on the basis of the oscillating output of said oscillator, as a reference clock signal, and said starter being arranged to have its operation controlled in accordance with the oscillating operation of said oscillator.

35. An electronic circuit according to Claim 32, further including: an oscillator responsive to the voltage, which is supplied from said second capacitor, as the power supply voltage; a frequency divider responsive to the output signal of said oscillator; and an oscillation detector for

detecting the oscillating operation of said oscillator, said starter including a latch circuit arranged to be rendered to a first state by the output signal of said oscillation detector, when the power supply is connected, and to a second state by the signal, which is thereafter fed out of said frequency divider.

36. An electronic circuit according to Claim 35, further including a voltage regulator responsive to the voltage, which is supplied to said second node, in order to supply a constant voltage to be supplied to said oscillator and said frequency divider.

37. An electronic circuit according to Claim 36, further including an output buffer circuit responsive to the voltage, which is supplied to said first node, as the power supply voltage.

38. An electronic circuit according to Claim 37: wherein said first to fourth switching elements, said clock generator, said starter, said oscillator, said frequency divider, said oscillation detector, said voltage regulator and said output buffer circuit are formed in a complementary type insulated gate field effect semiconductor integrated circuit device; and wherein said first and second capacitors are connected to said complementary type insulated gate field effect semiconductor integrated circuit device.

39. An electronic circuit according to Claim 38, wherein said first node is supplied with the voltage of a battery.

40. An electronic circuit according to Claim 39, wherein said battery is a lithium battery.

41. An electronic watch powered by an electronic circuit according to any one of the preceding claims.

42. An electronic circuit constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figs. 1 to 9, or Fig. 10, or Fig. 11, or Fig. 14, or Fig. 16, or Fig. 20, or Fig. 21 of the accompanying drawings.

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